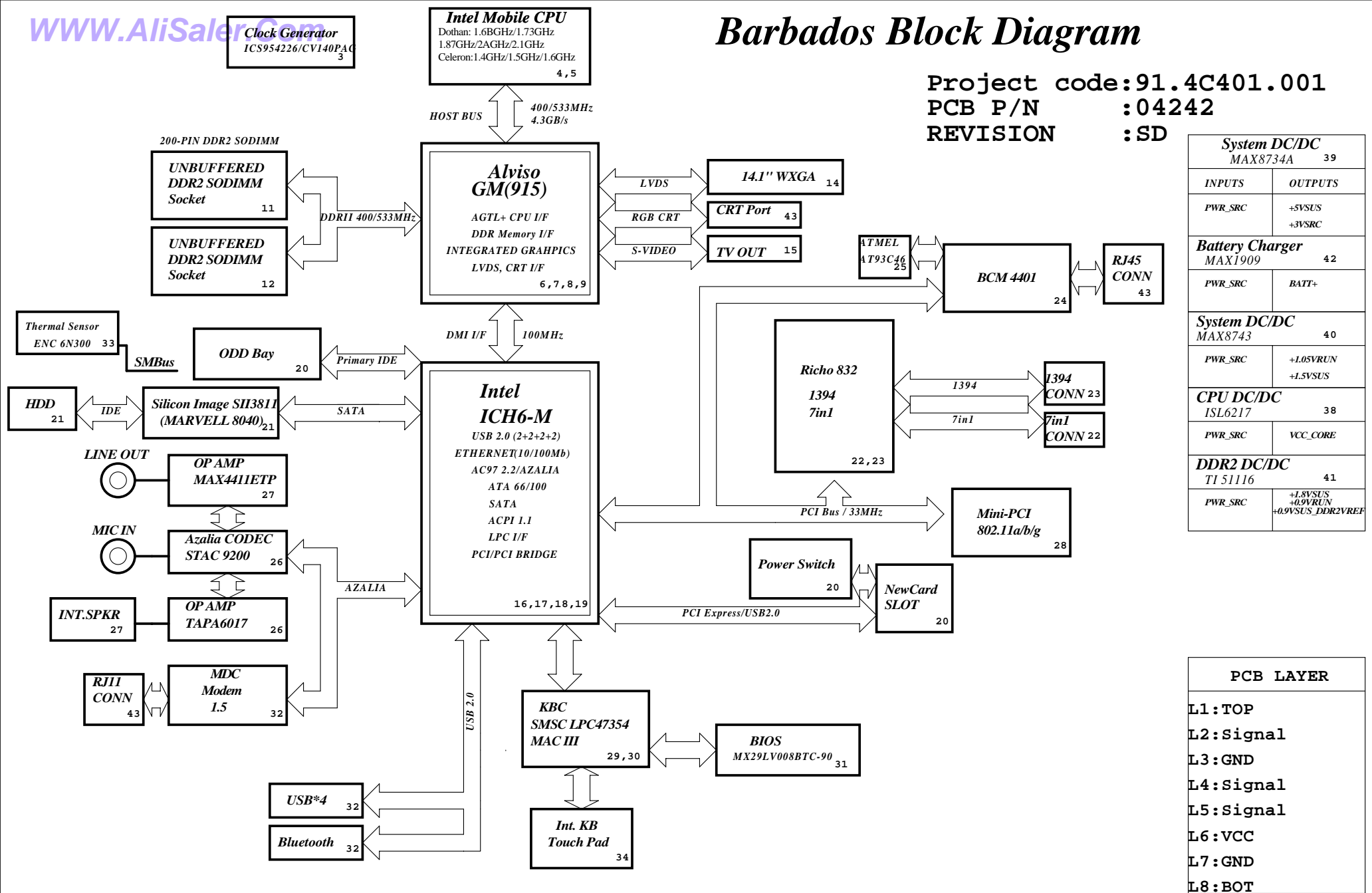


Barbados Block Diagram

Project code: 91.4C401.001
PCB P/N : 04242
REVISION : SD



Wistron/Dell confidential

<Core Design>

DELL		Wistron Corporation	
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Title: Block diagram			
Size: Custom	Document Number: Barbados	Rev: SD	
Date: Thursday, May 12, 2005	Sheet: 1	of	44

Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration page 7
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK in signal.

ICH6-M Strapping Signals and Configuration

Pin Name	Strap Description	Note
ACZ_SDOUT	0=Normal(default) 1=XOR Test mode	
ACZ_SYNC	0=Normal(default)	1=Reserved
DPRSLPVR	0=Normal	1=Reserved
EE_CS	0=Normal	1=Reserved
EE_DOUT	0=Normal	1=Reserved
GNT[5]#/GPO[17]#	0=PCI cycles to FWH 1=PCI cycles to LPC (default)	Selects memory range to FWD to out of PCI
GNT(6)#/GPO(16)#	0="Top block swap" mode 1=Normal(default)	"Top block swap" inverts A16 on cycles to FWH
GPIO[25]	0=Internal 2.5V DISEN(default) 1=ENABLE Internal Vcc2_5VVRM	
INTVRMEN	0=Internal VccSus1.5V DISEN (default) 1=ENABLE Internal VccSus1.5VVRM	
LINKALERT#	1=Normal(requires external PU)	0=Reserved
REQ[4:1]	XOR Test Chain Selection	Requires external resistors
SATALED#	0=Normal(default)	1=Reserved
SPKR	0=Normal(default) 1=NO Reboot	
TP[3]	0=Enter XOR Test mode 1=Normal(default)	

NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWOK signal.

BATT+ BATT+ 42,43
DC_IN+ DC_IN+ 42,43,44
PWR_SRC PWR_SRC 14,29,38,39,40,41,42,43,44
VCCRTC VCCRTC 16,18,29,33

+0.9VSUS_DDR2VREF +0.9VSUS_DDR2VREF 7,11,12,41,44
+5VSUS +5VSUS 18,26,27,32,33,36,39,40,41,43,44
+3VSUS +3VSUS 14,17,18,19,20,24,25,27,28,32,33,35,36,39,40,41,43,44
+1.5VSUS +1.5VSUS 18,36,40,44

For Dothan B stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
LAN Broadcom BCM4401/BCM5507	AD16	PIRQC#	REQ4# / GNT4#
MINIPCI SLOT	AD19	PIRQB# PIRQD#	REQ3# / GNT3#
R5C832	AD17	PIRQA# PIRQC#	REQ1# / GNT1#

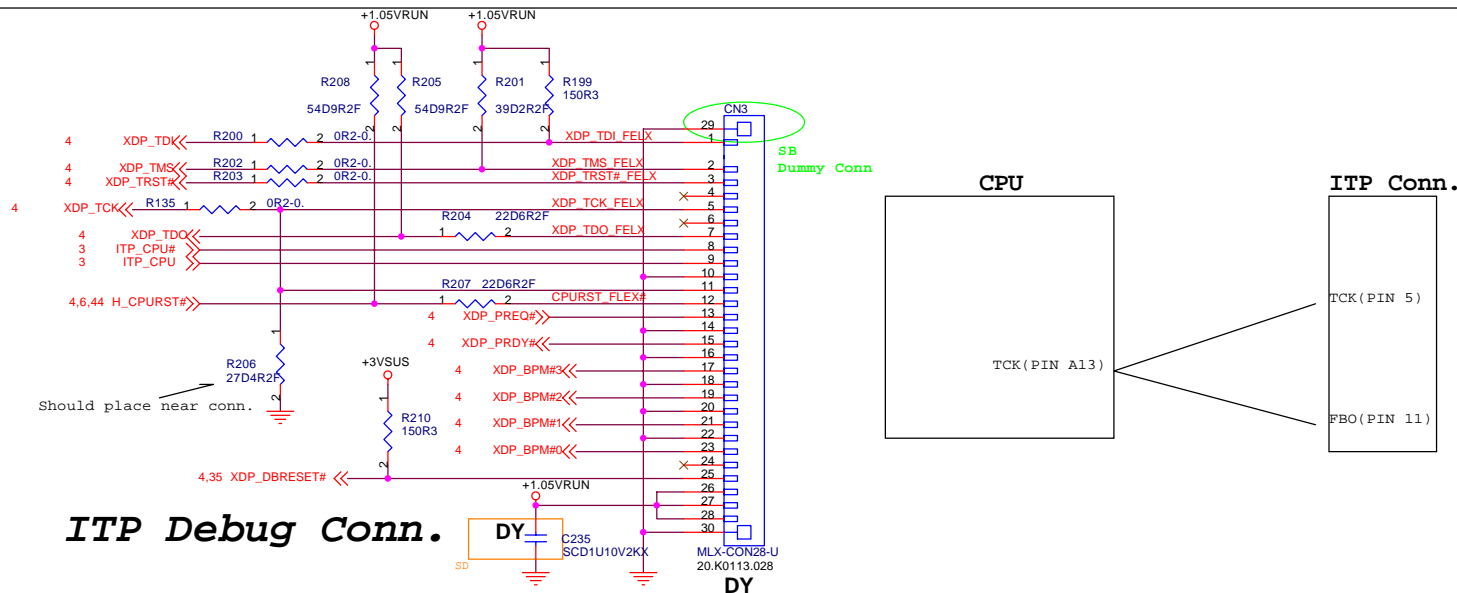
ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------



+2.5VRUN +2.5VRUN 7,9,14,15,18,36,43,44
+5VRUN +5VRUN 14,15,18,20,21,26,28,30,33,34,36,38,43,44
+12V +12V 14,23,33,36,43,44
+1.5VRUN +1.5VRUN 5,7,9,17,18,20,36,44
VCC_CORE VCC_CORE 5,36,38,44
+1.05VRUN +1.05VRUN 3,4,5,6,7,9,10,16,18,33,36,40,44
LCDVDD LCDVDD 14,44
+3VRUN +3VRUN 3,4,9,11,12,14,15,17,18,19,20,21,22,23,26,27,28,29,30,32,33,35,36,38,43,44

+5VALW +5VALW 14,30,36,39,43,44
+3VALW +3VALW 4,14,20,22,29,30,31,33,34,39,43,44

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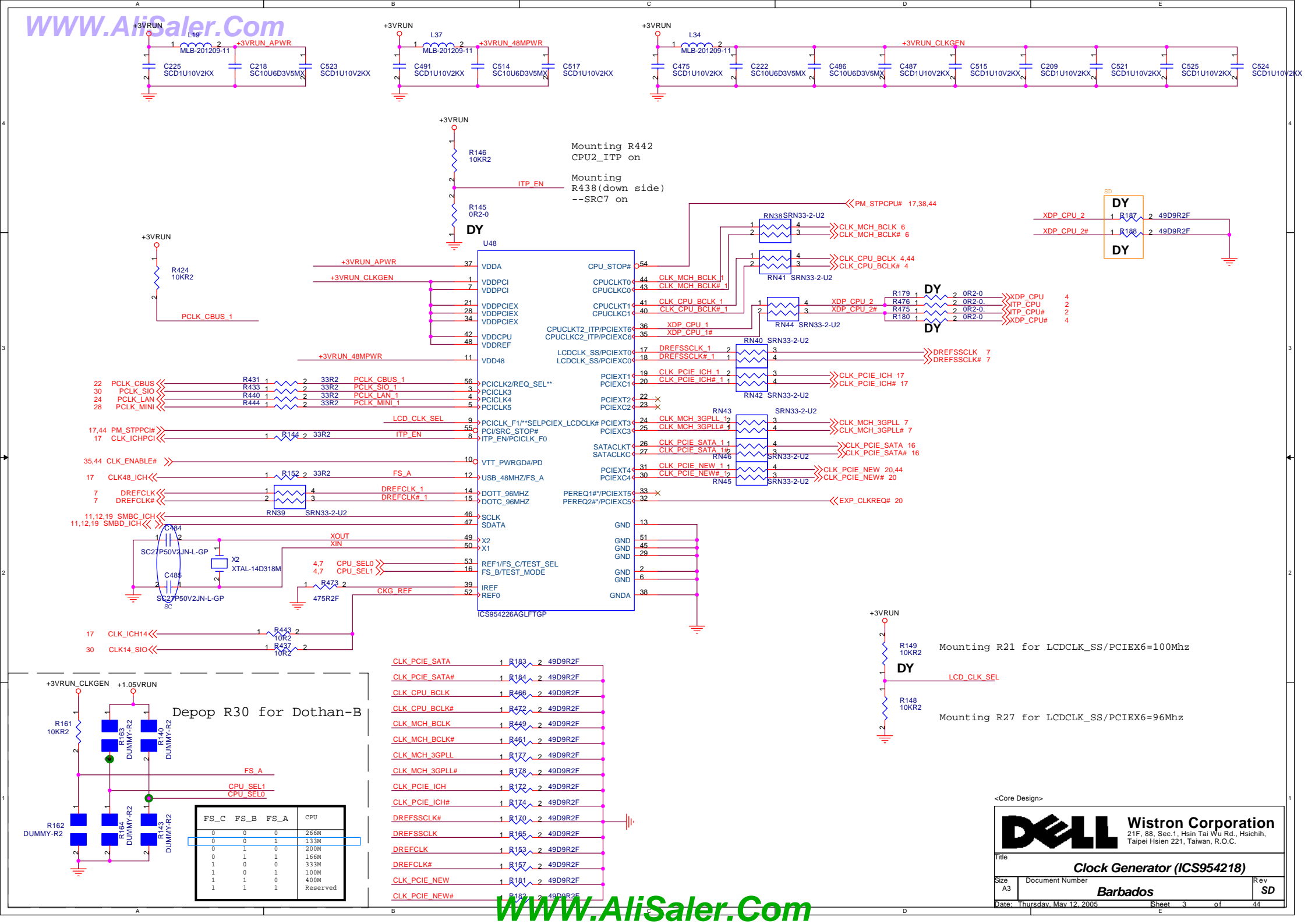
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

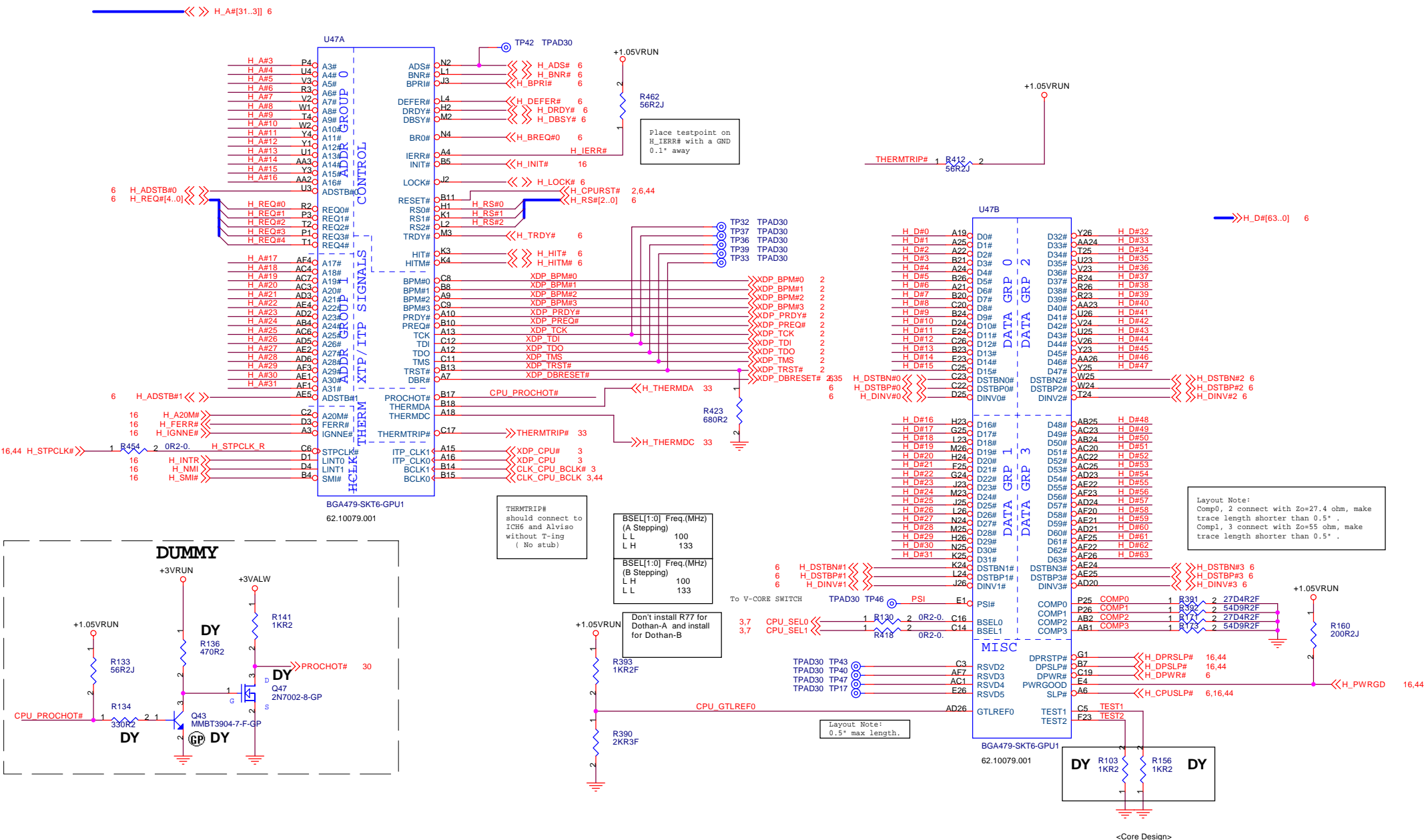
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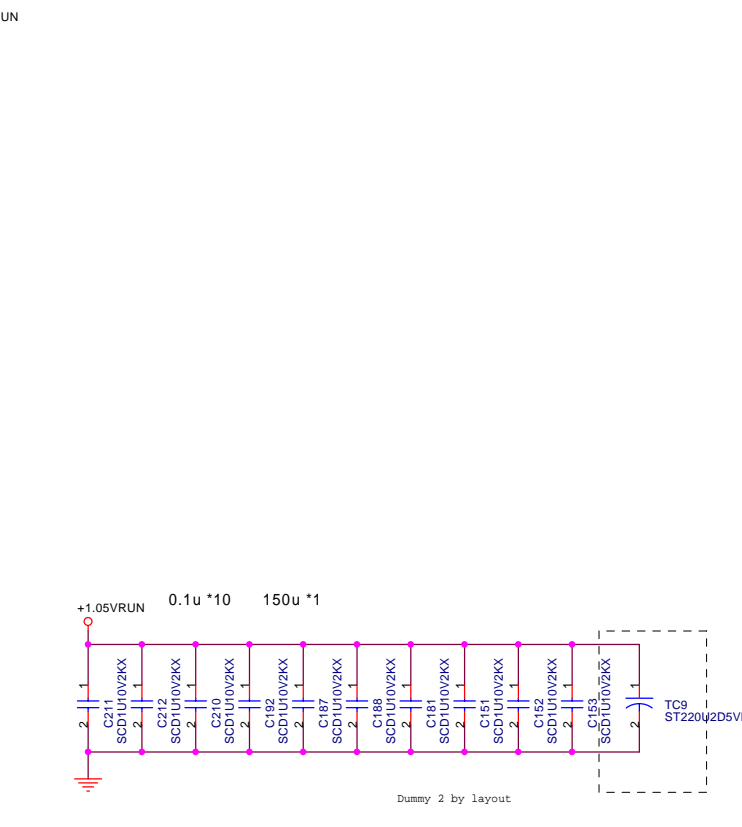
Size A3 Document Number **Barbados** Rev SD

Date: Thursday, May 12, 2005 Sheet 2 of 44

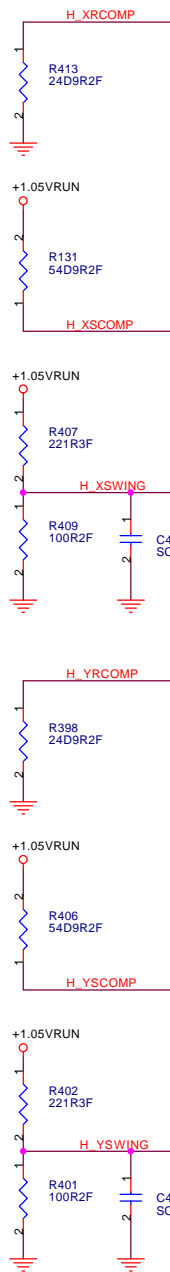
WWW.AliSaler.Com



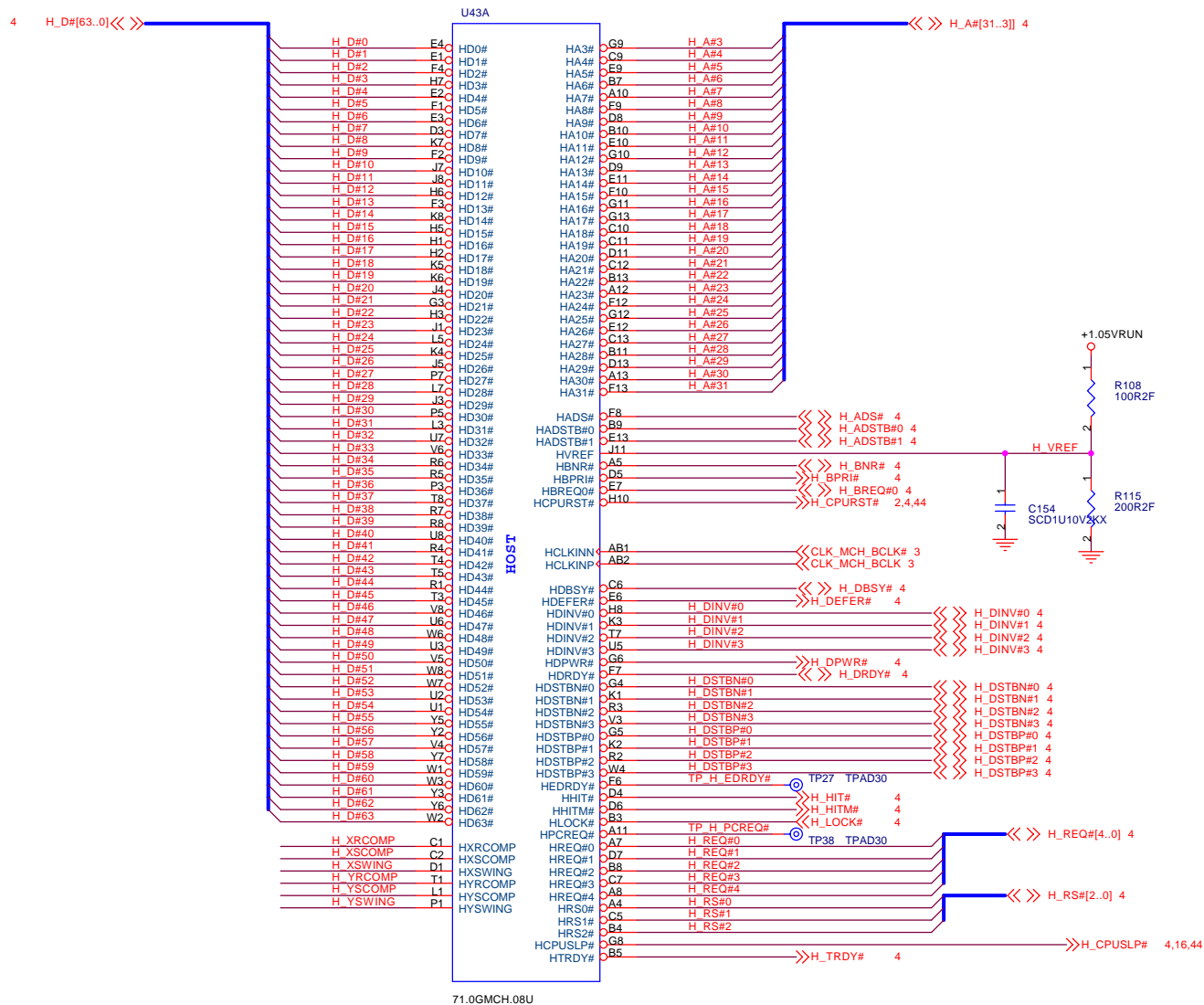


[illegible]

U47D		
A2	VSS0	D13
A5	VSS1	D15
A8	VSS2	D17
A11	VSS3	D19
A14	VSS4	D21
A17	VSS5	D23
A20	VSS6	D26
A23	VSS7	E3
A26	VSS8	E6
AA1	VSS9	E8
AA4	VSS10	E10
AA6	VSS11	E12
AA8	VSS12	E14
AA10	VSS13	E16
AA12	VSS14	E18
AA14	VSS15	E20
AA16	VSS16	E22
AA18	VSS17	E25
AA20	VSS18	F1
AA22	VSS19	F4
AA25	VSS20	F5
AB3	VSS21	F7
AB5	VSS22	F9
AB7	VSS23	F11
AB9	VSS24	F13
AB11	VSS25	F15
AB13	VSS26	F17
AB15	VSS27	F19
AB17	VSS28	F21
AB19	VSS29	F24
AB21	VSS30	G2
AB23	VSS31	G6
AB26	VSS32	G23
AC2	VSS33	G22
AC5	VSS34	G26
AC8	VSS35	H3
AC10	VSS36	H5
AC12	VSS37	H21
AC14	VSS38	H25
AC16	VSS39	J1
AC18	VSS40	J4
AC21	VSS41	J6
AC24	VSS42	J22
AD1	VSS43	J24
AD4	VSS44	K2
AD7	VSS45	K5
AD9	VSS46	K21
AD11	VSS47	K23
AD13	VSS48	K26
AD15	VSS49	L3
AD17	VSS50	L6
AD19	VSS51	L22
AD22	VSS52	L25
AD25	VSS53	M1
AE3	VSS54	M4
AE6	VSS55	M5
AE8	VSS56	M21
AE10	VSS57	M24
AE12	VSS58	N3
AE14	VSS59	N6
AE16	VSS60	N22
AE18	VSS61	N23
AE20	VSS62	N26
AE23	VSS63	P2
AE26	VSS64	P5
AF2	VSS65	P21
AF5	VSS66	P24
AF11	VSS67	R1
AF13	VSS68	R4
AF15	VSS69	R6
AF17	VSS70	R22
AF19	VSS71	R25
AF21	VSS72	T3
AF24	VSS73	T5
B3	VSS74	T21
B6	VSS75	T23
B9	VSS76	T26
B12	VSS77	U2
B16	VSS78	U6
B19	VSS79	U21
B22	VSS80	U24
B25	VSS81	V1
C1	VSS82	V4
C4	VSS83	V5
C7	VSS84	V21
C10	VSS85	V25
C13	VSS86	W3
C15	VSS87	W6
C18	VSS88	W22
C21	VSS89	W23
C24	VSS90	W26
D2	VSS91	Y2
D5	VSS92	Y5
D7	VSS93	Y21
D9	VSS94	Y24
D11	VSS95	
	VSS96	



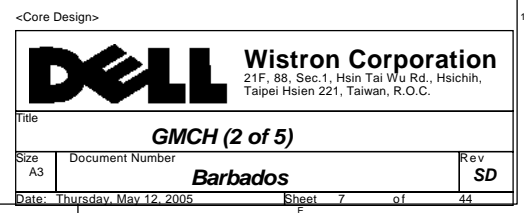
Place them near to the chip

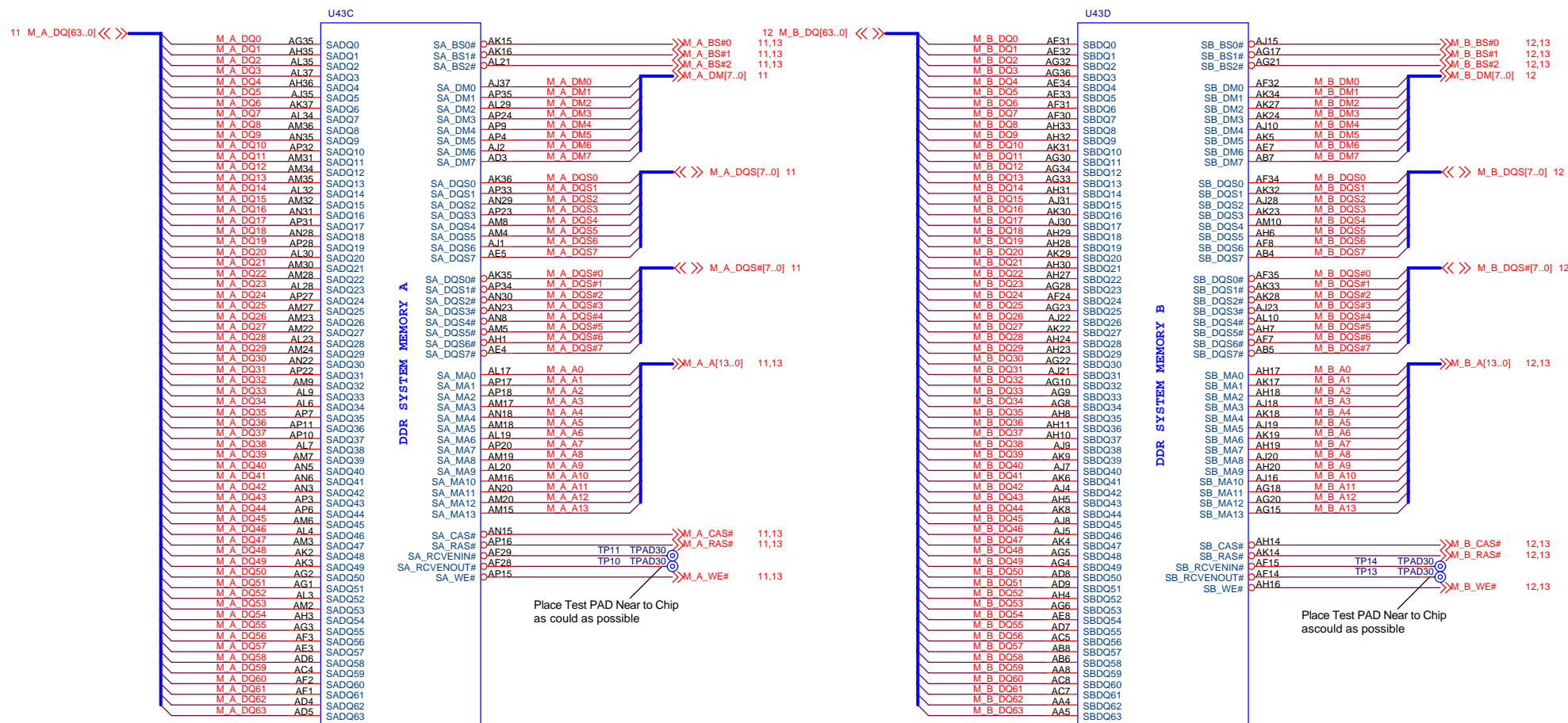


71.0GMCH.08U

<Core Design>

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Title GMCH (1 of 5)		
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71.0GMCH.08U

71.0GMCH.08U

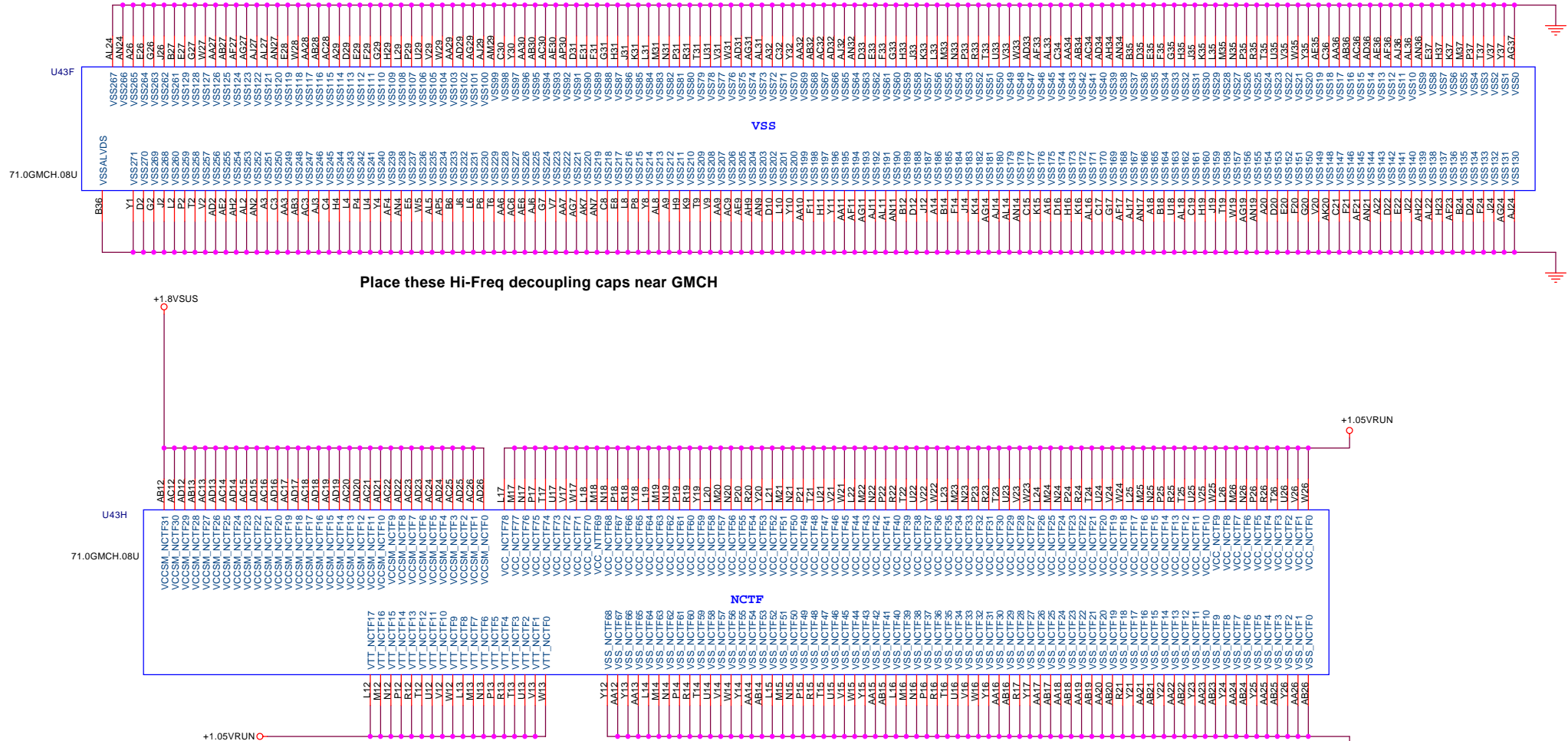
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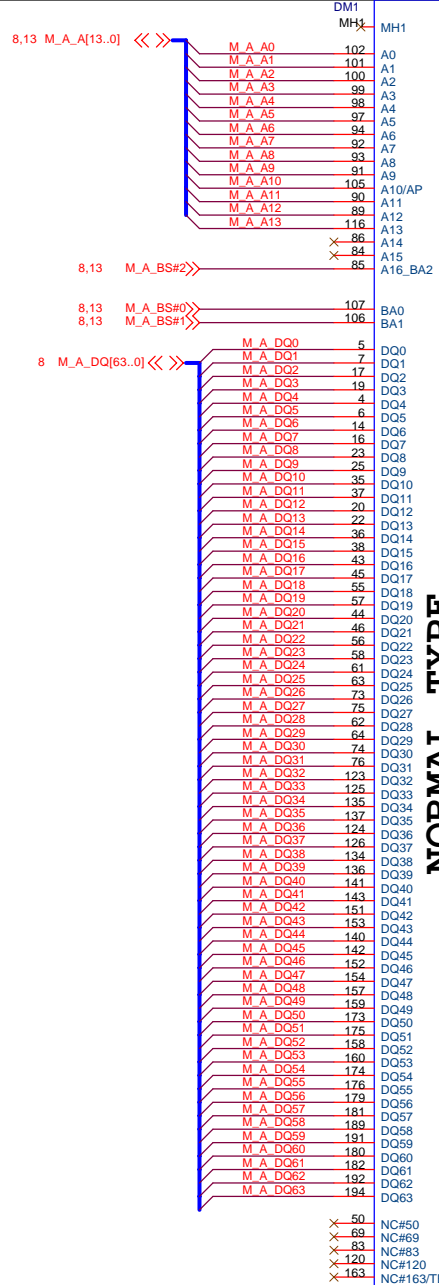


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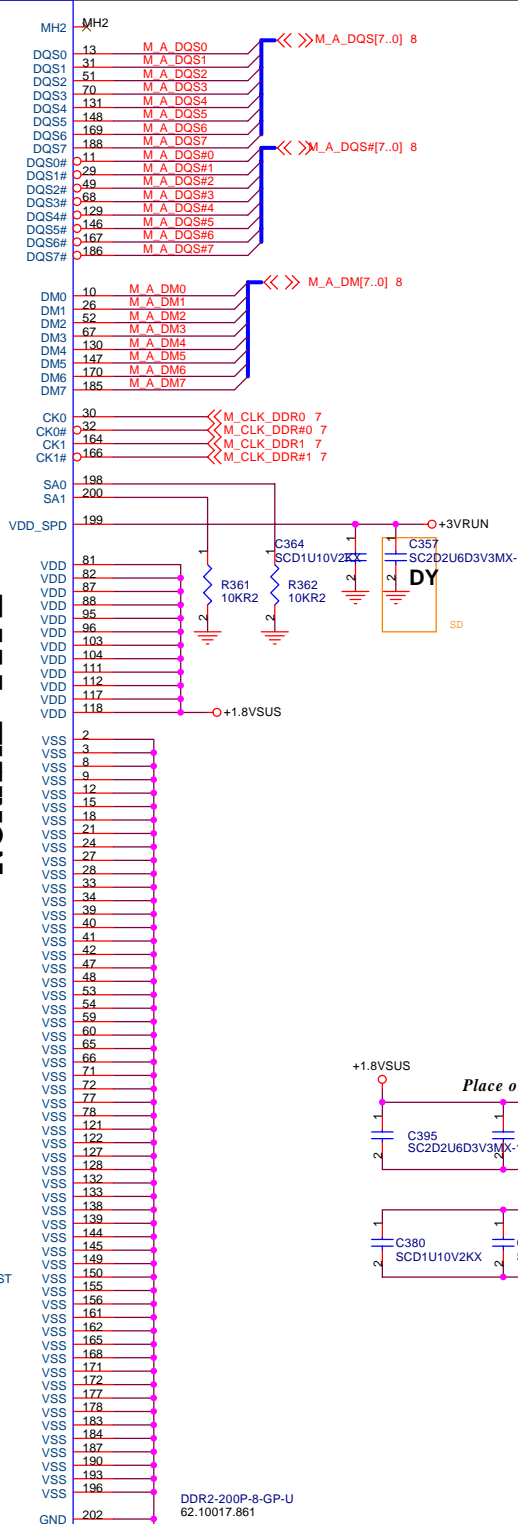
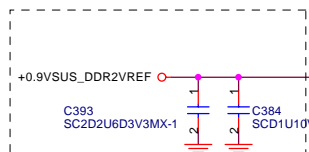
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Size	Document Number	Rev			
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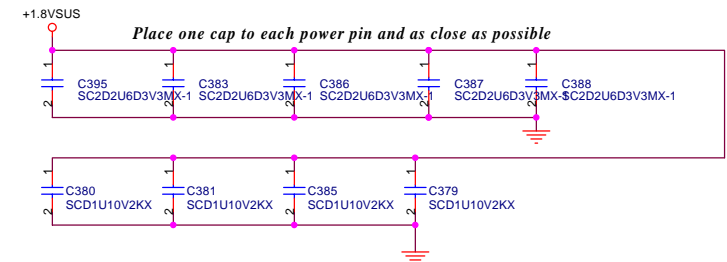
Please close to Pin 1 as close as possible



(REVERSE TYPE)
DIMM 2(BOT side)

ALVISO
(BOT side)

(Normal Type)
DIMM 1(Top side)

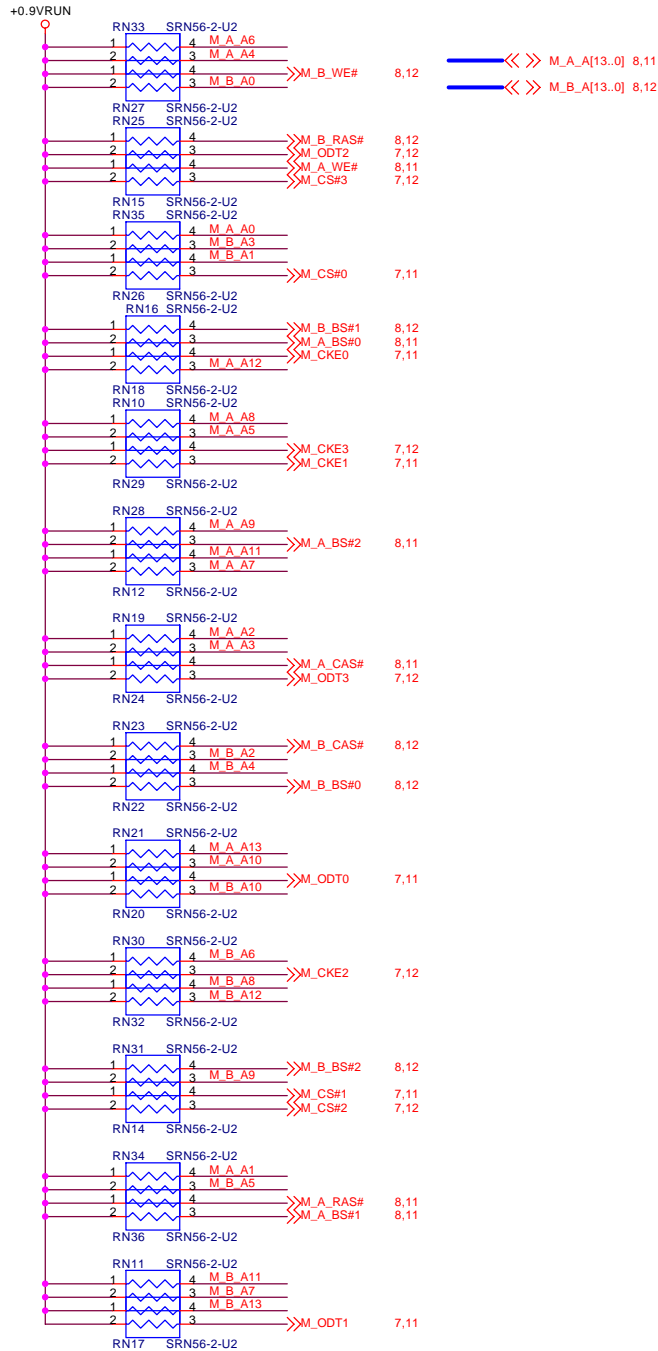


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DELL		Wistron Corporation	
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Title DDR-2 SO-DIMM A			
Size A3	Document Number Barbados		Rev SD
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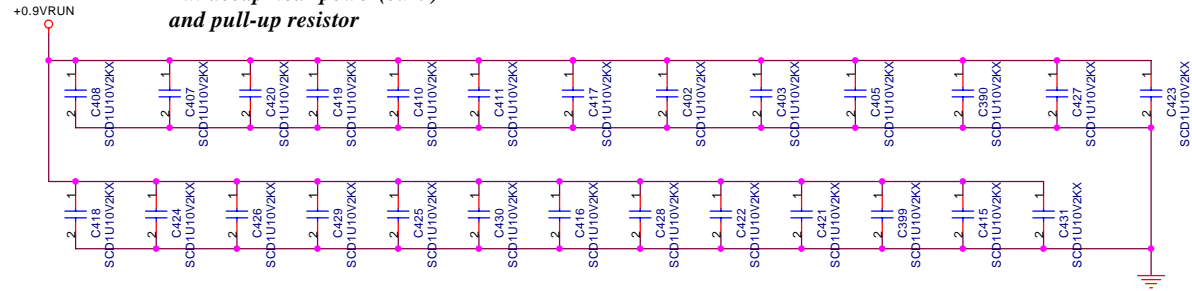


Put decap near power(0.9V) and pull-up resistor



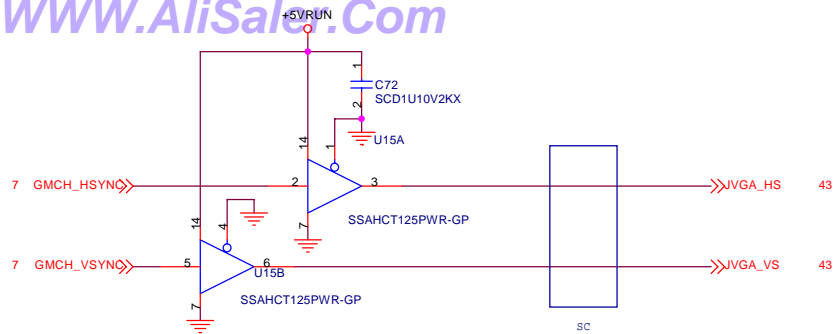
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

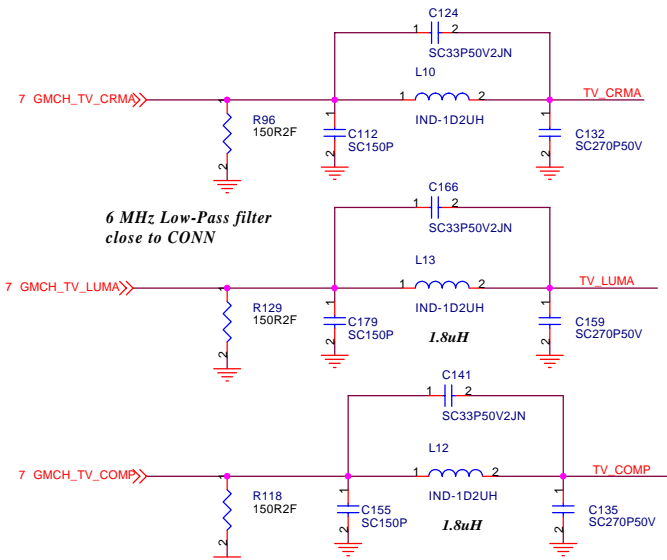
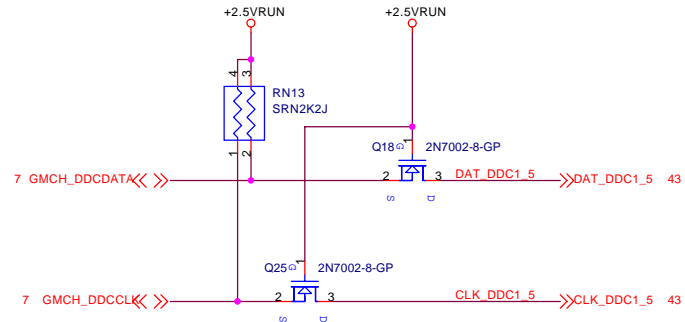


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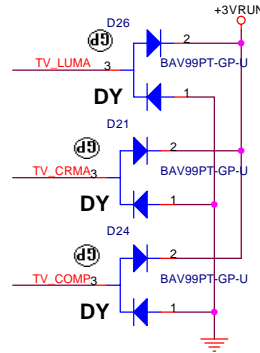
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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DDR-2 TERMINATION / STRAPS			
Size A3	Document Number	Rev	
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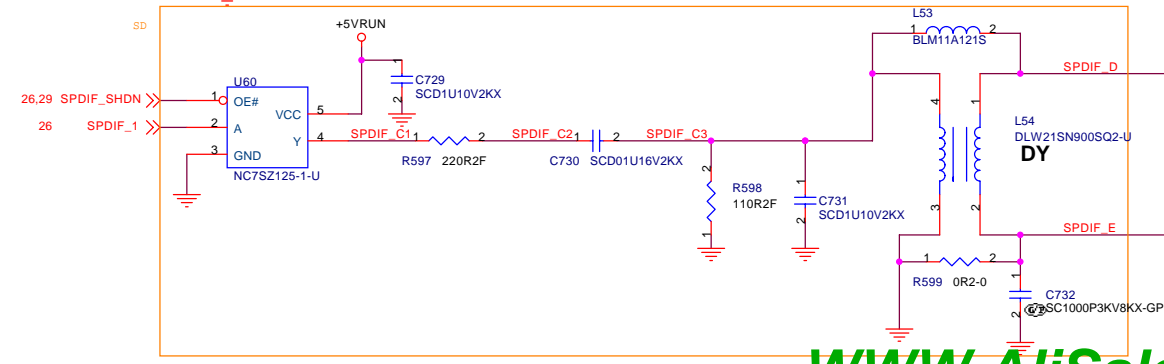
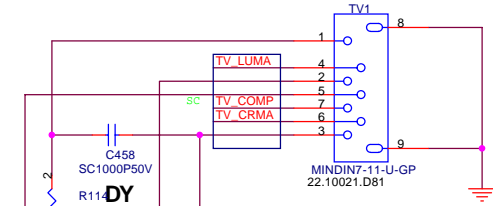
DDC_CLK & DATE LEVEL SHIFT



ESD Protection Diode



TVOUT CONN

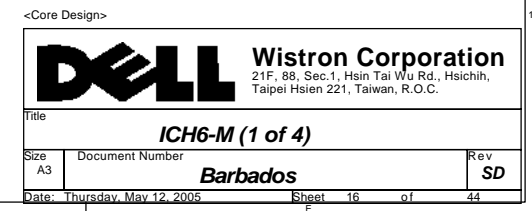


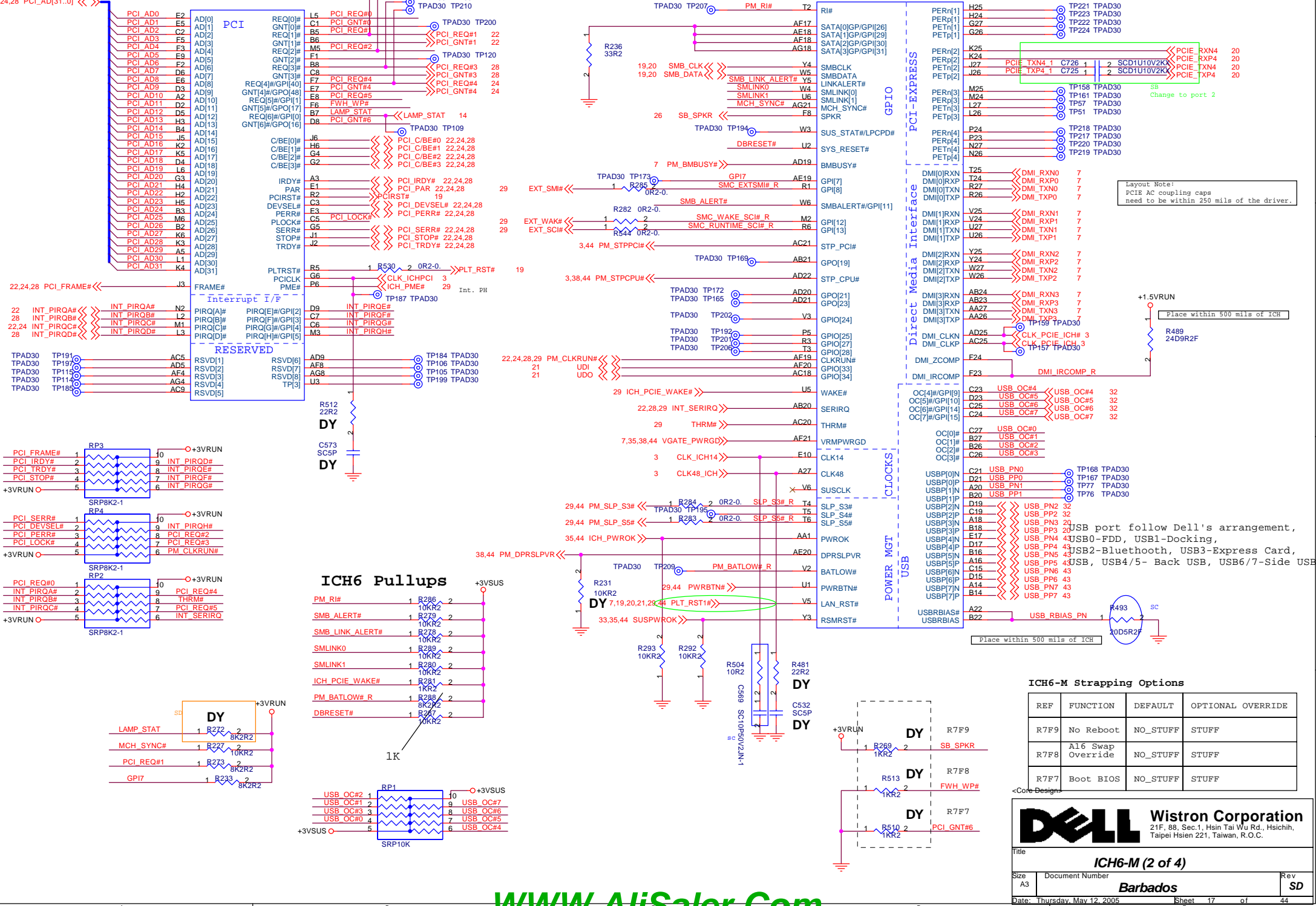
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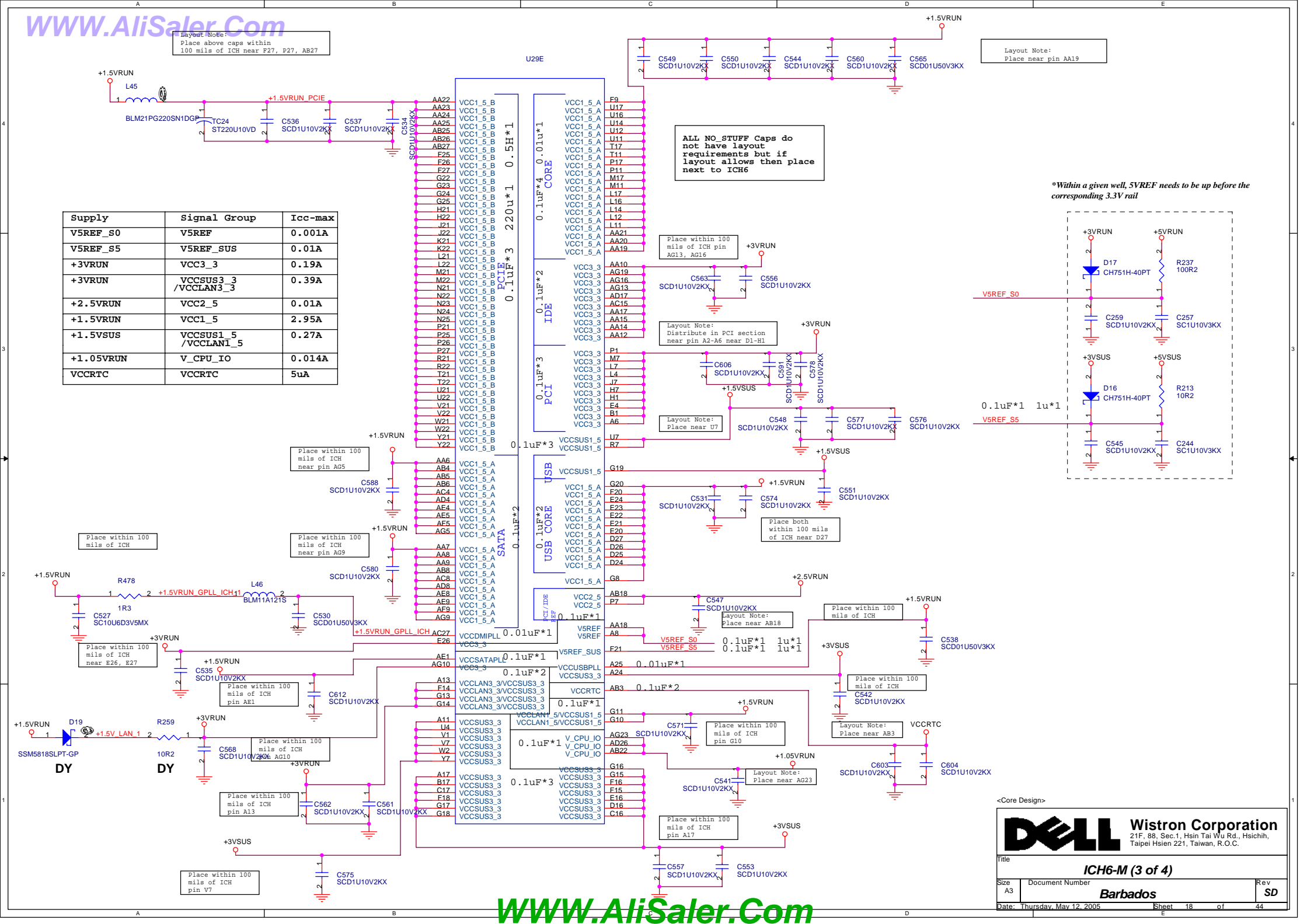
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Title		TV CONN.	
Size	Document Number	Rev	SD
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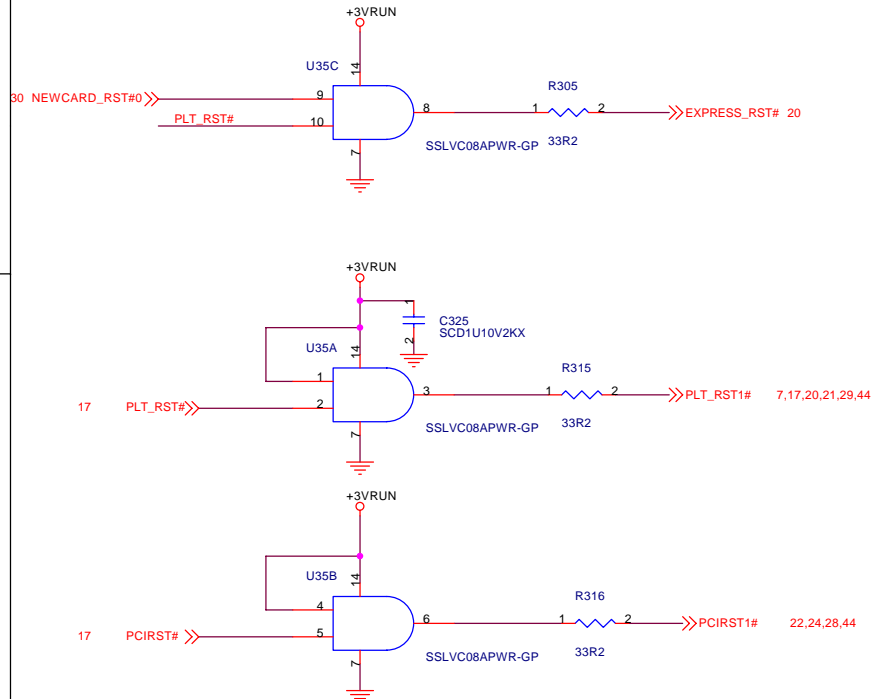
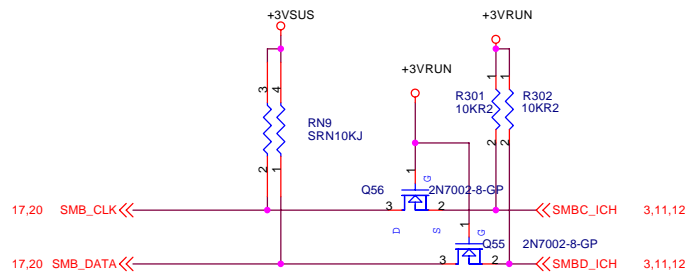




Supply	Signal Group	Icc-max
V5REF_s0	V5REF	0.001A
V5REF_s5	V5REF_SUS	0.01A
+3VRUN	VCC3_3	0.19A
+3VRUN	VCCSUS3_3 /VCCLAN3_3	0.39A
+2.5VRUN	VCC2_5	0.01A
+1.5VRUN	VCC1_5	2.95A
+1.5VSUS	VCCSUS1_5 /VCCLAN1_5	0.27A
+1.05VRUN	V_CPU_IO	0.014A
VCCRTC	VCCRTC	5uA



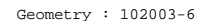
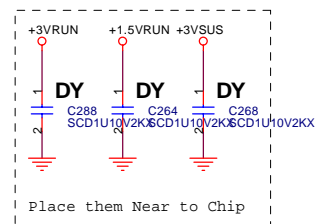
SMBUS



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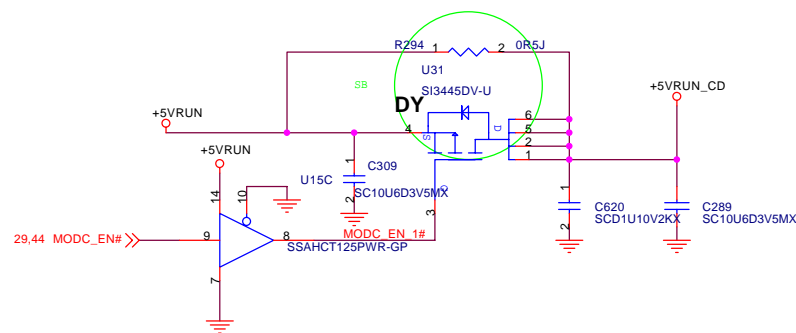
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Title ICH6-M (4 of 4)		
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For Newcard socket

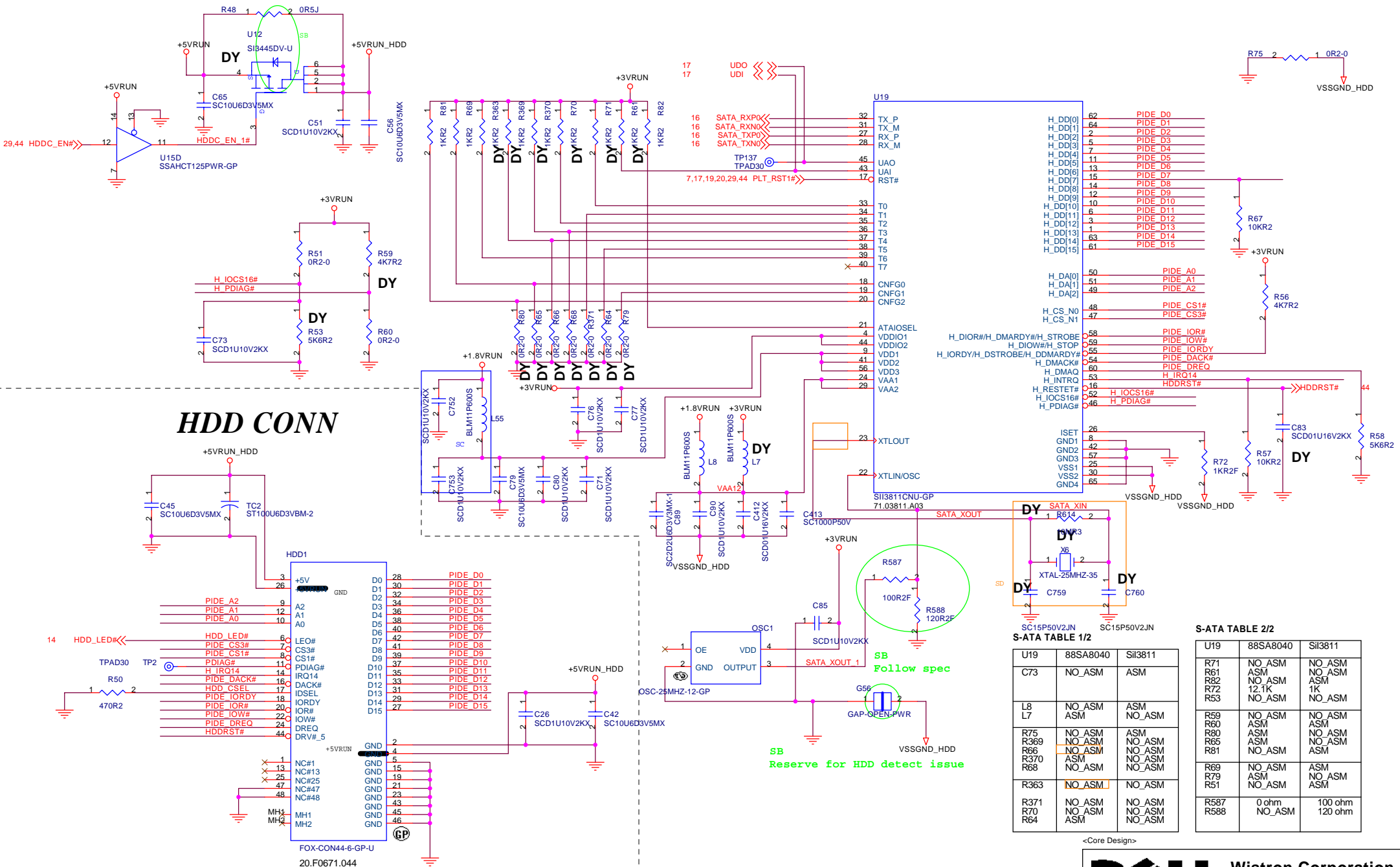
Reserve the symbol
for TOP side
connector

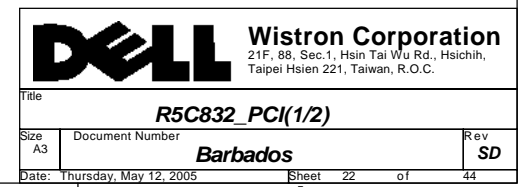


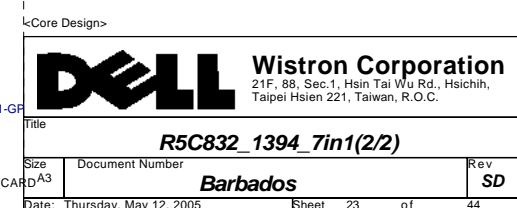
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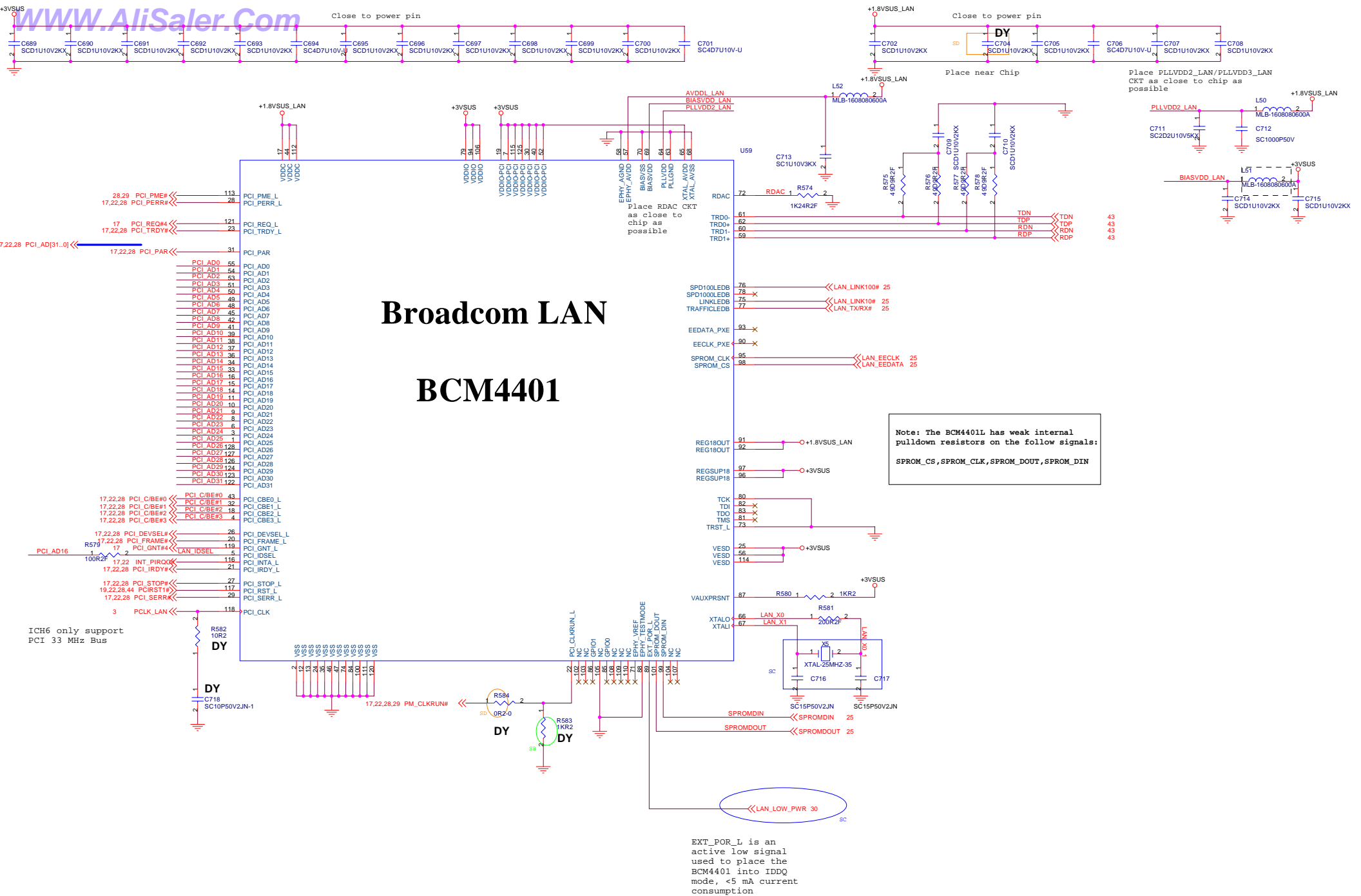


Title			
CDROM/NEWCARD			
Size A3	Document Number	Rev	
	Barbados	SD	
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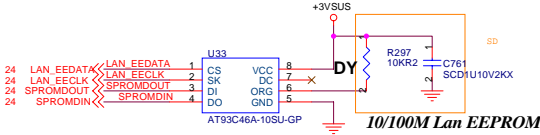




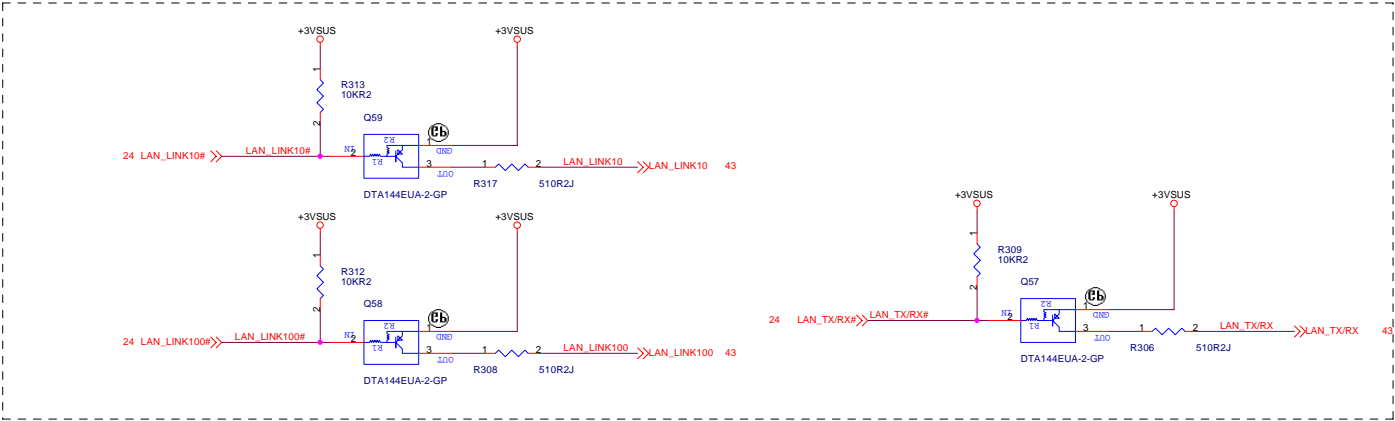


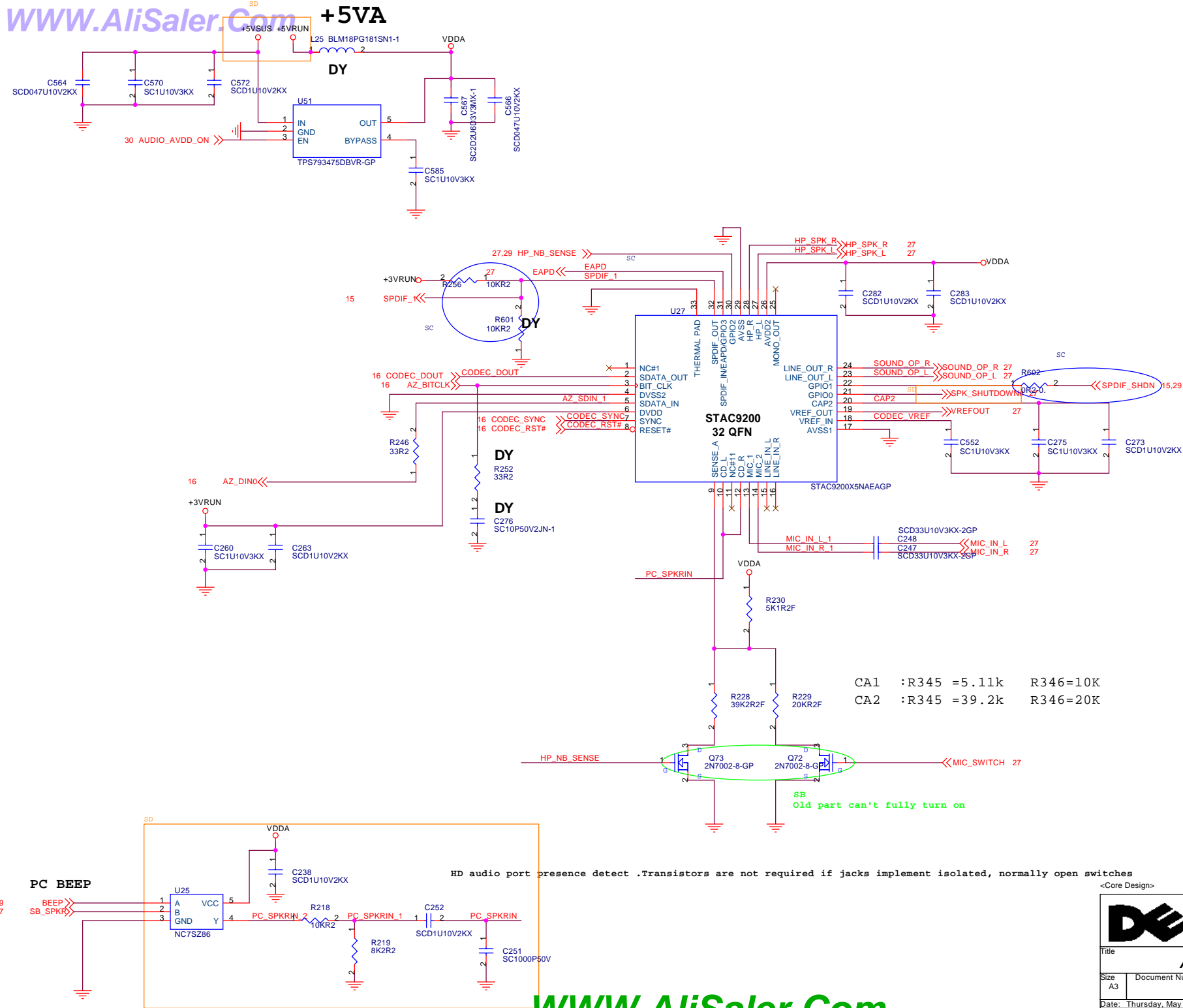
Broadcom LAN

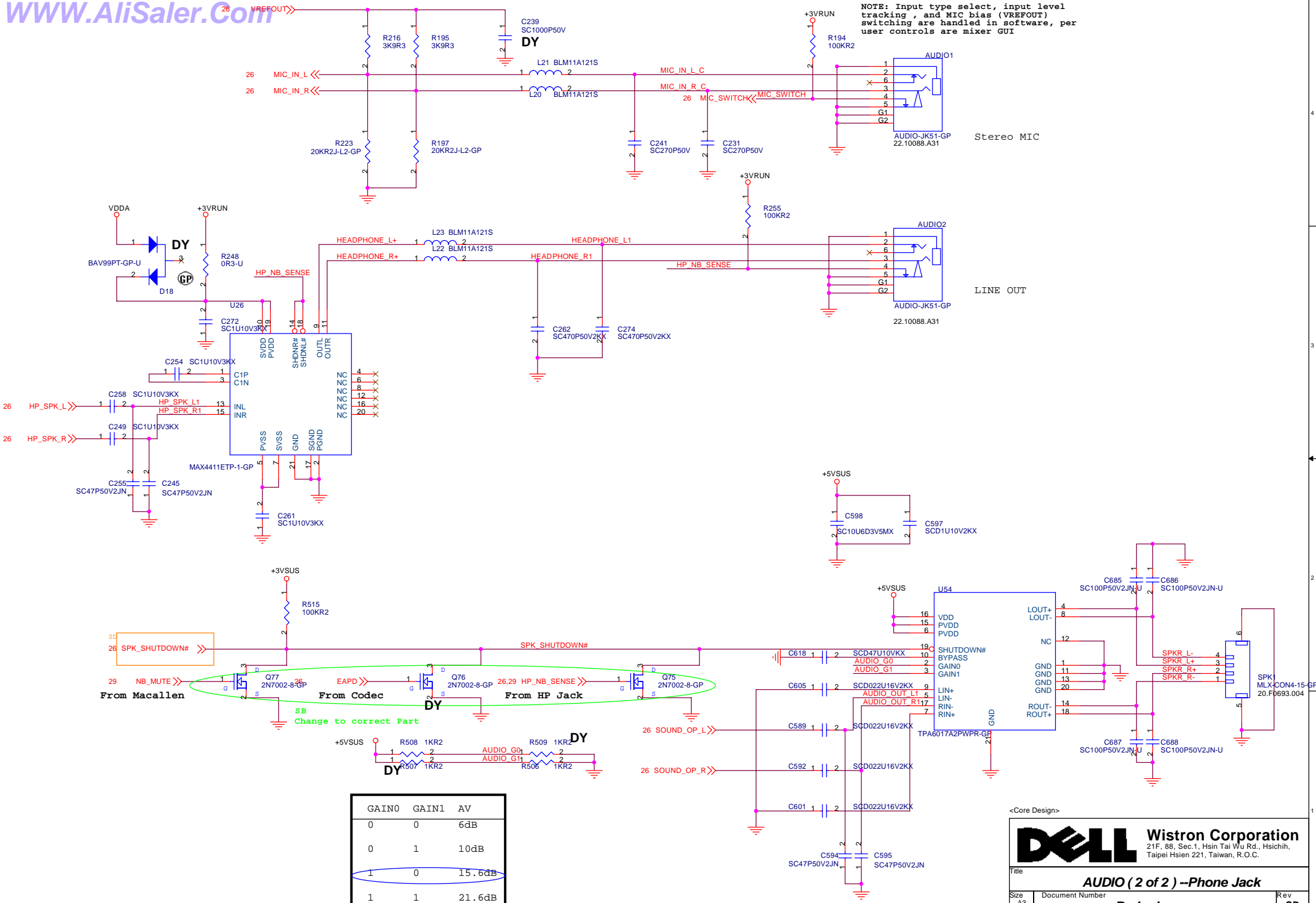
BCM4401

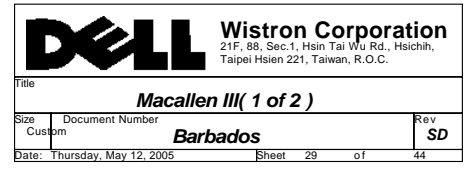


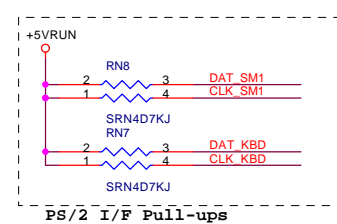
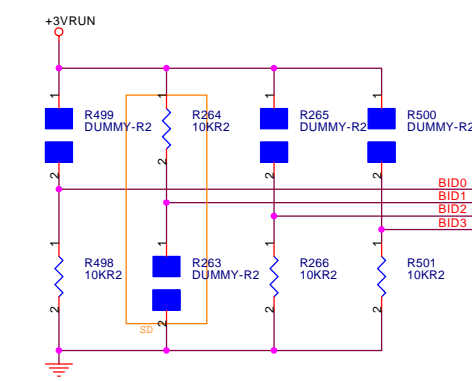
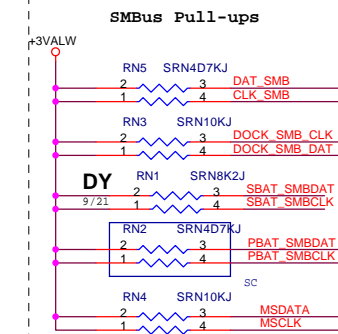
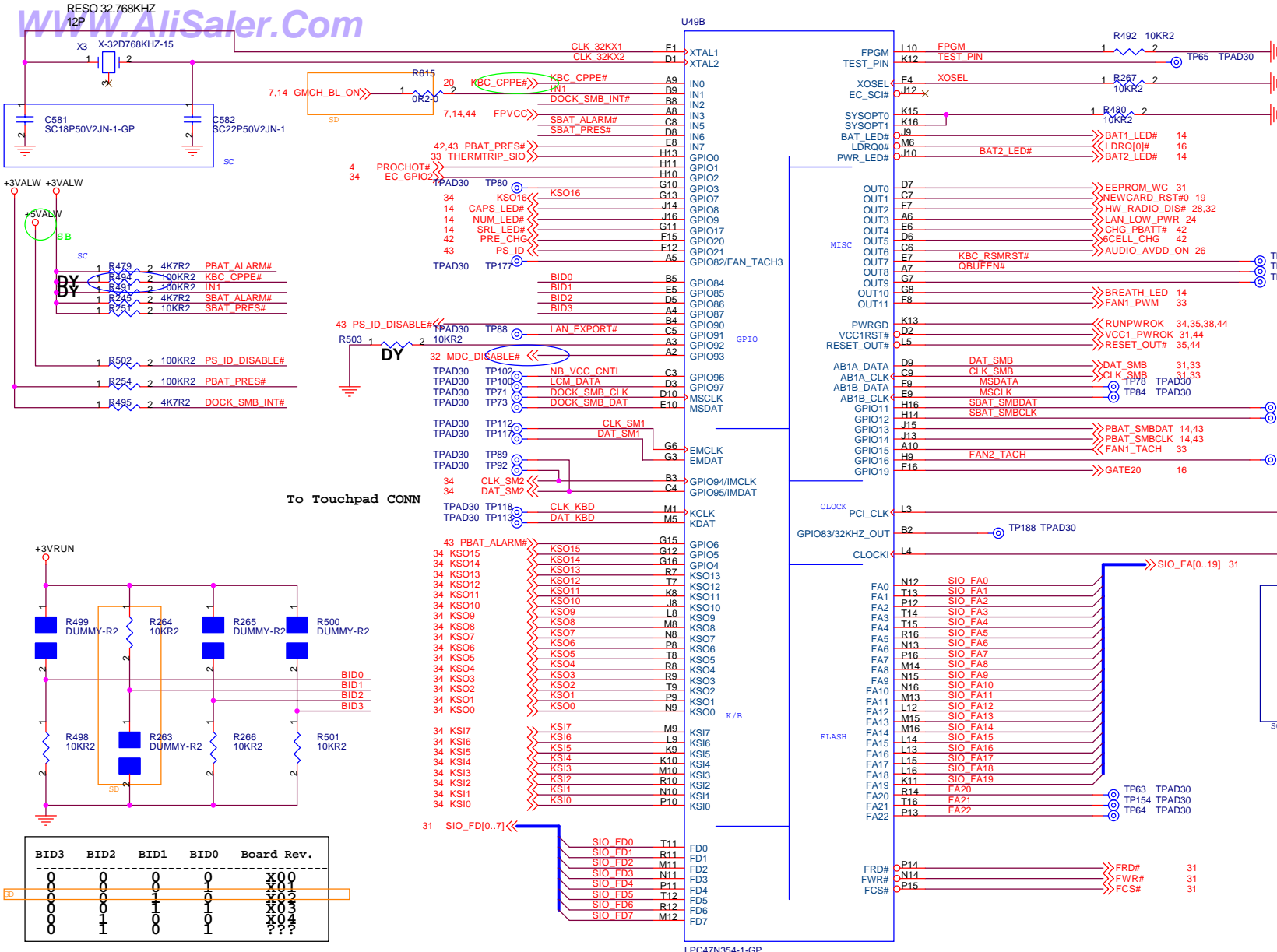
Atmal: AT93C46-10SI "72.93C46.K01" (Main source)
ST : M93C46-W "72.93C46.E01" (2nd source)











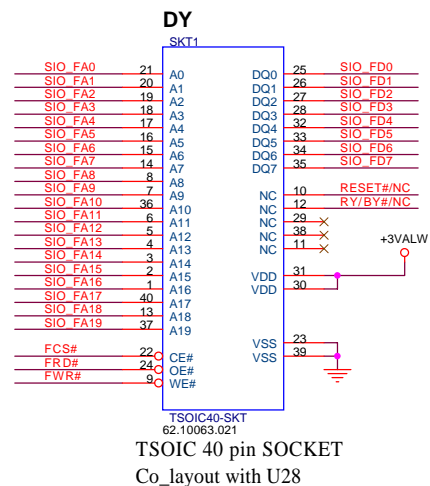
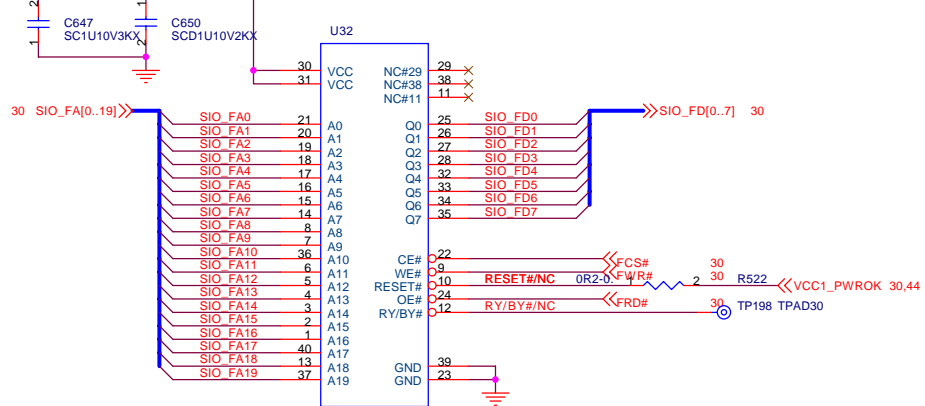
KSO_17 and KSI0 for i button
 KSO_17 and KSI6 for Audio_Mute# button
 KSO_17 and KSI4 for Volum Up button
 KSO_17 and KSI5 for Volum down button

<Core Design>

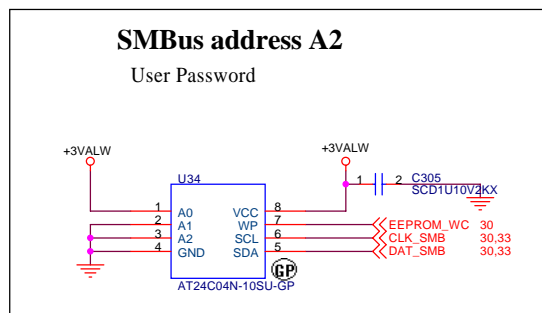
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Macallen III(2 of 2)**

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Barbados		
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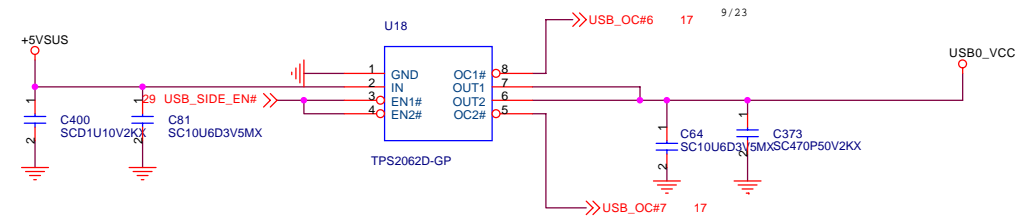
MXIC: MX29LV008CTTI-90G "72.29008.G09" (Main sorce,LF,bottom boot block)
ST: M29W008AB-90 "72.29008.C09" (2nd sorce)



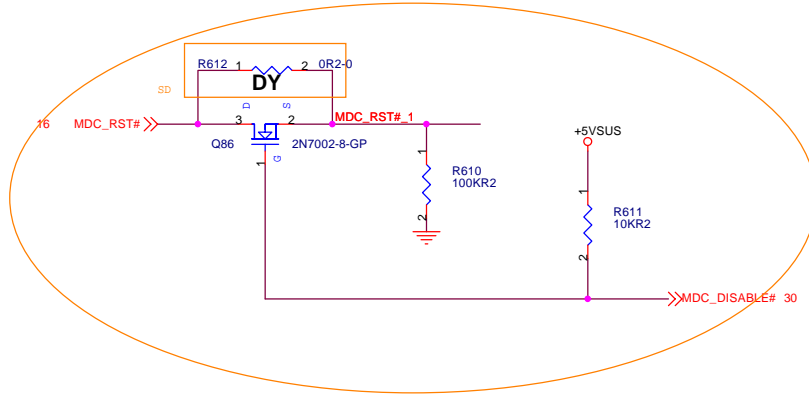
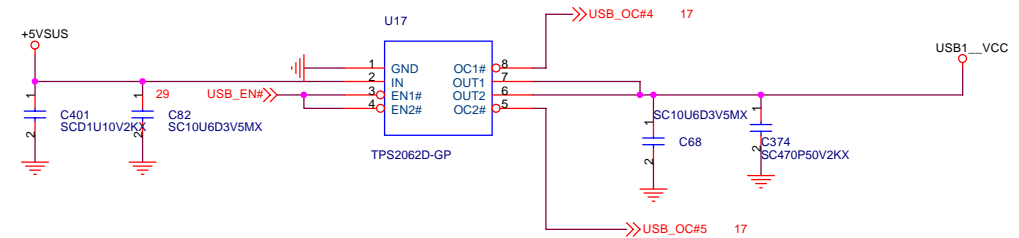
Atmel: AT24C04N-10SI "72.24C04.D01" (Main sorce)
ST : M24C04 "72.24C04.B01" (2nd sorce)

<Core Design>

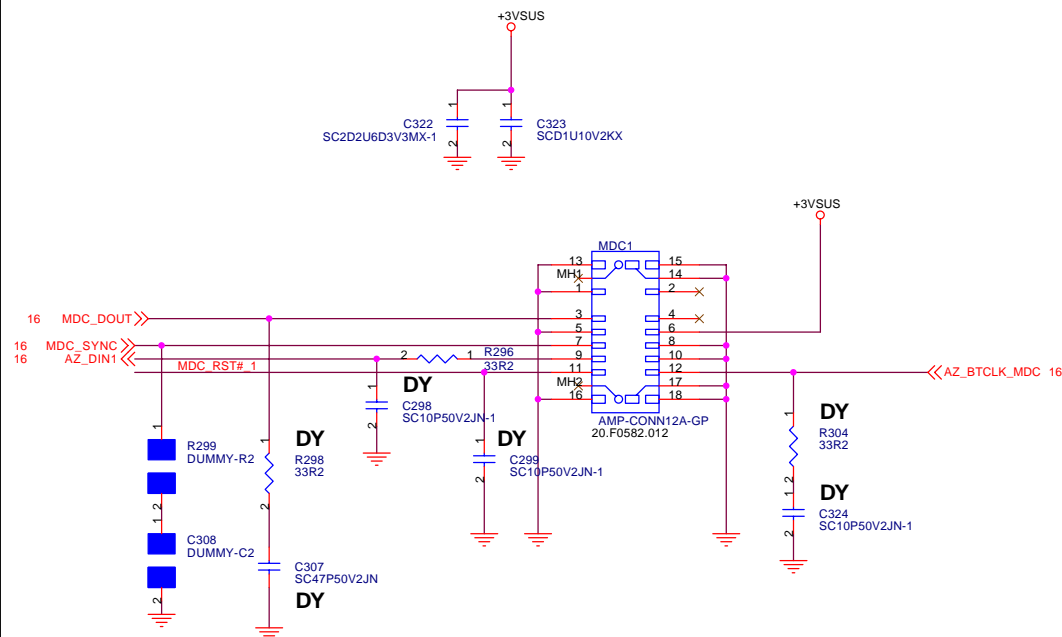
Dual USB0_VCC switch for USB6/USB7



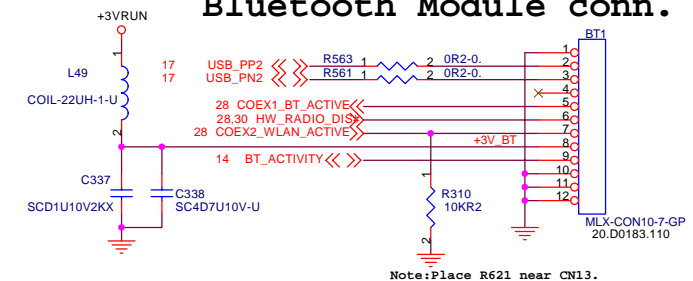
Dual USB1_VCC switch for USB4/USB5



Modem Connector (Not Standard Type)



Bluetooth Module conn.

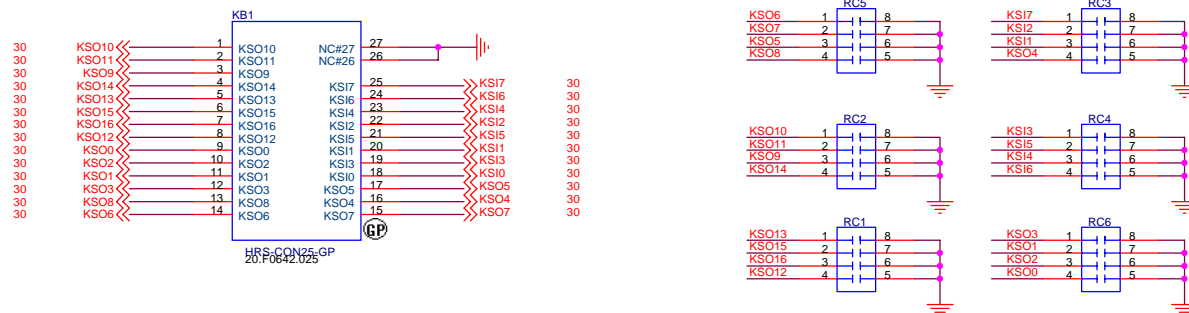


Note: Place R621 near CN13.

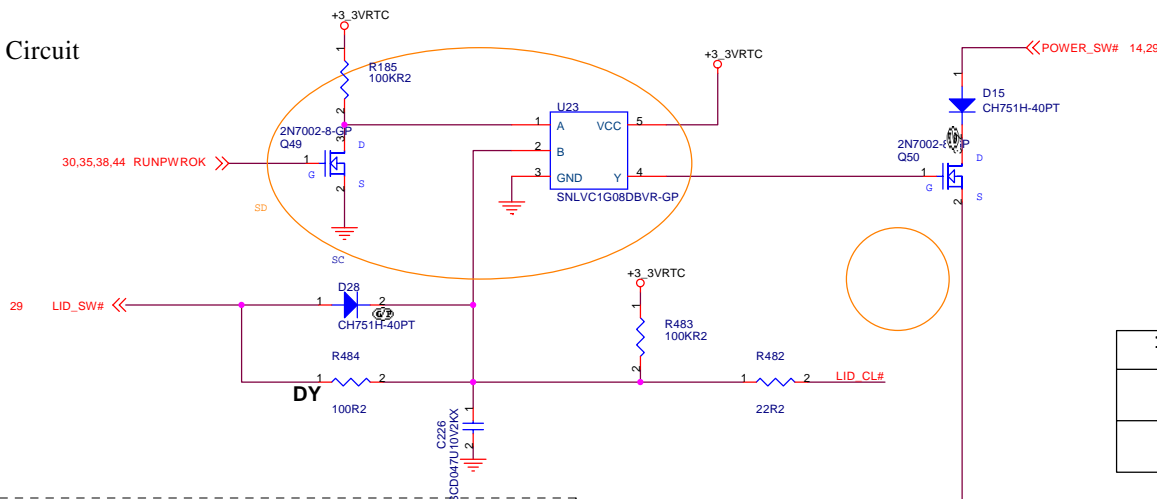
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DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB / MDC /BT/FIR			
Size A3	Document Number Barbados		Rev SD
Date:	Thursday, May 12, 2005	Sheet 32 of	44

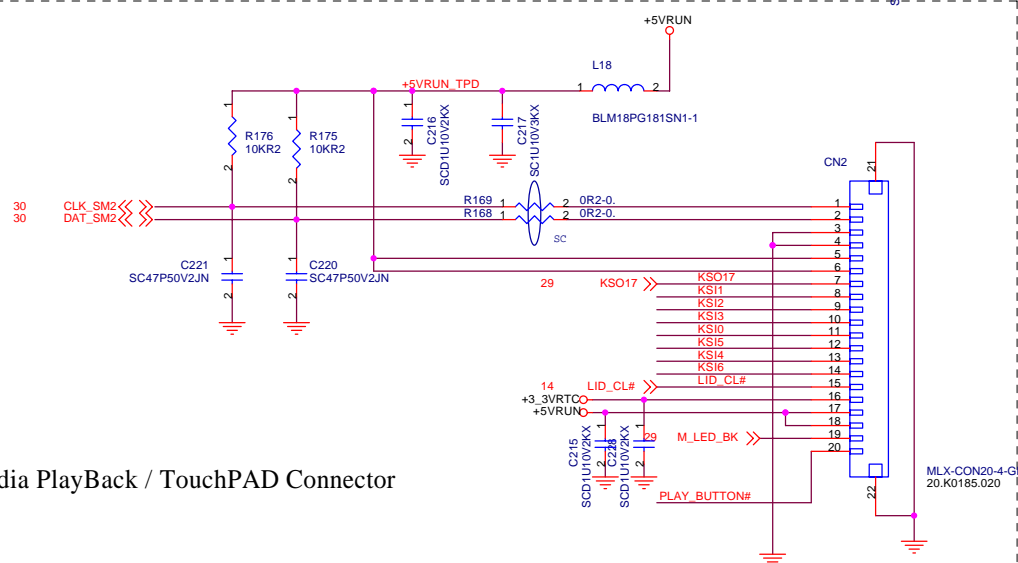
KB CONN



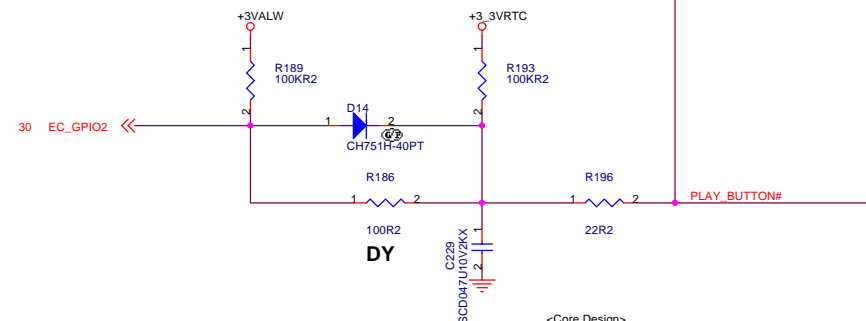
Instant ON Circuit



PLAY_PWR	PLAY_Button#
LOW	Regular Play Function
HIGH	Power On Function



Media PlayBack / TouchPAD Connector

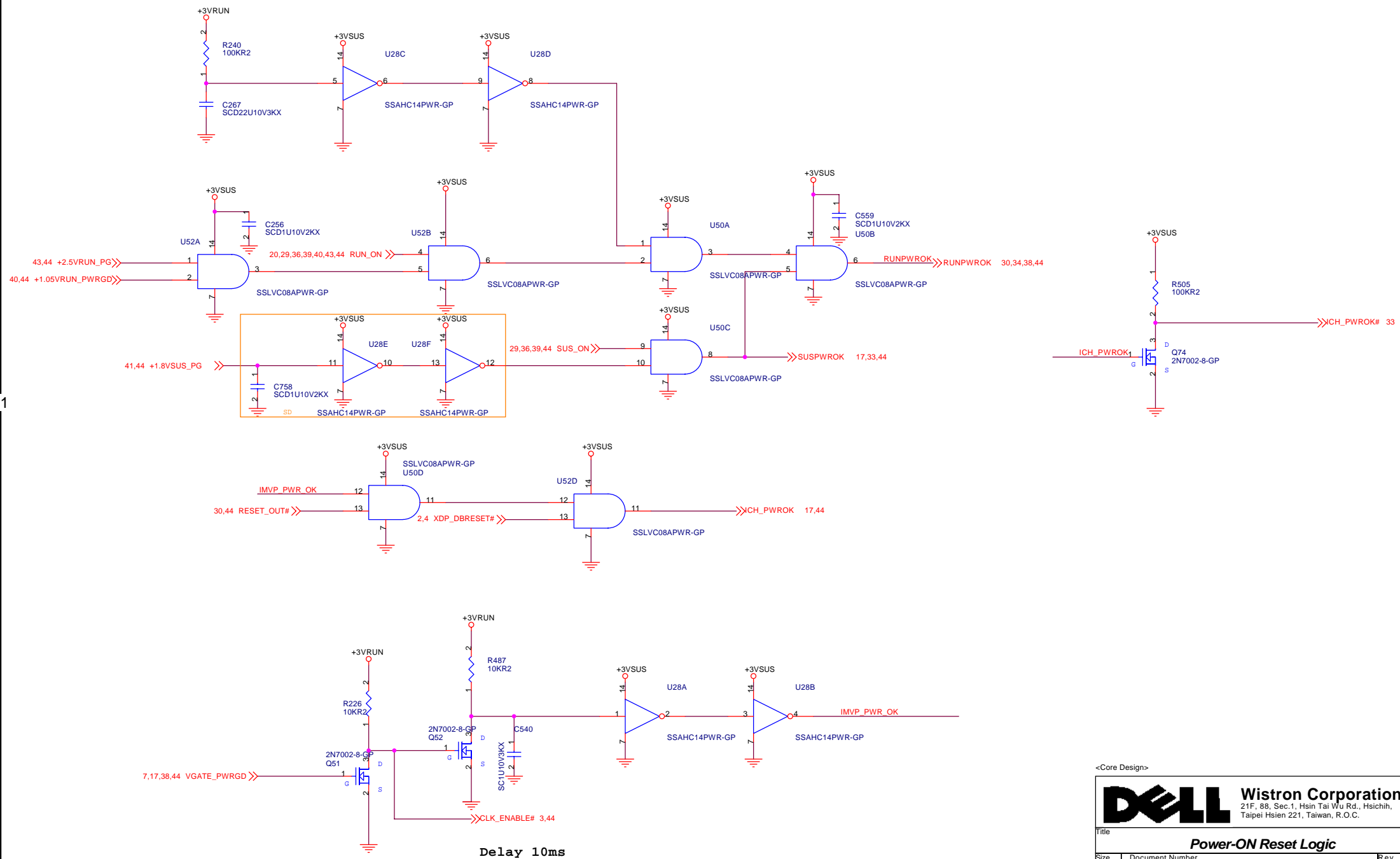


<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

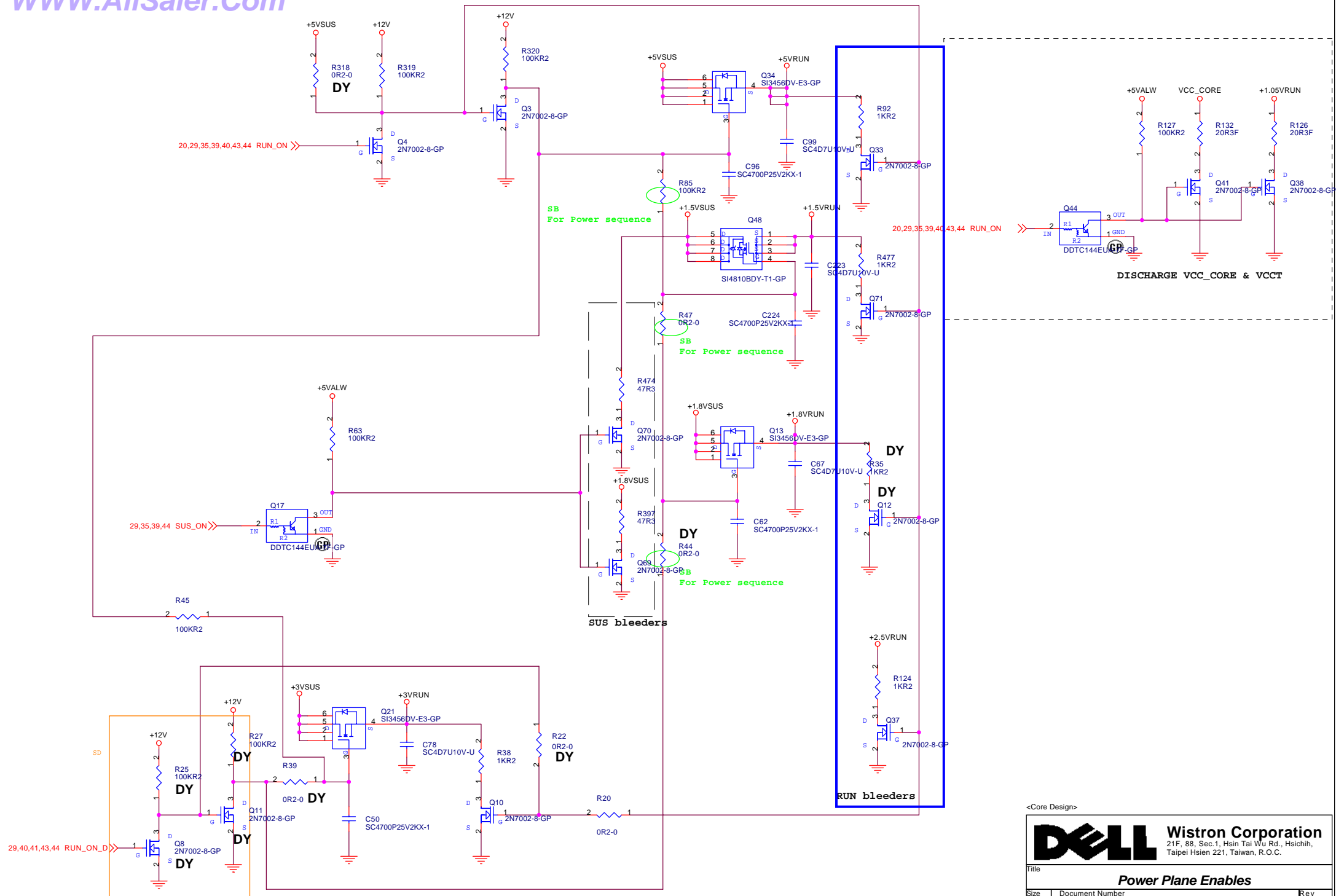
Title			
KB/TPAD/Media Playback Conn			
Size	Document Number	Rev	
Custom	Barbados	SD	
Date: Thursday, May 12, 2005	Sheet 34	of 44	




Delay 10ms

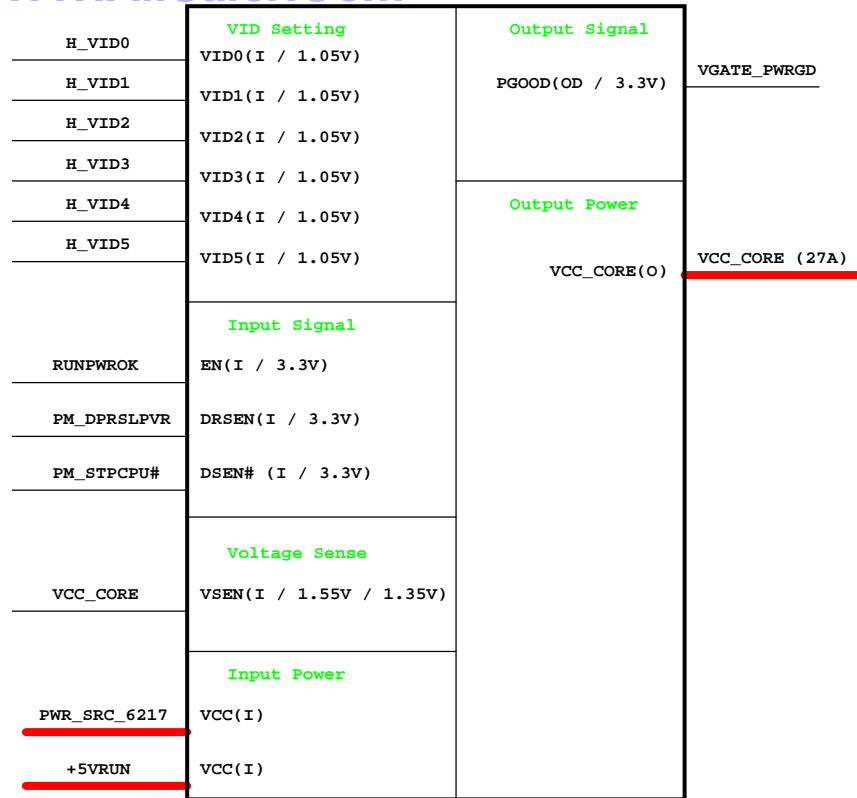
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DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Power-ON Reset Logic		
Size A3	Document Number Barbados	Rev SD
Date: Thursday, May 12, 2005 Sheet 35 of 44		

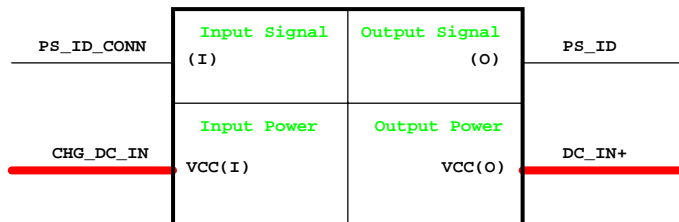


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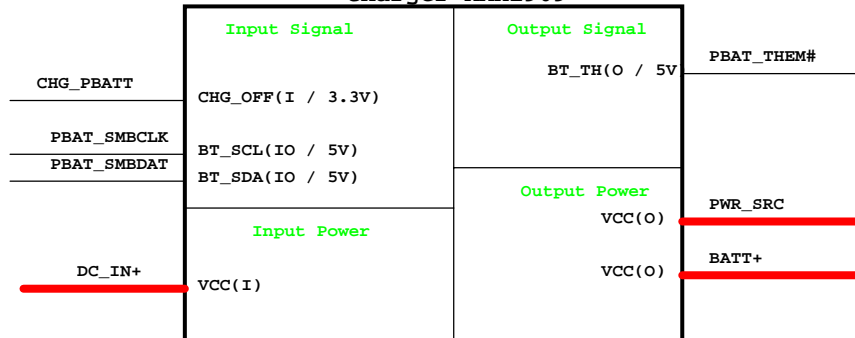
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Power Plane Enables</i>			
Size A3	Document Number <i>Barbados</i>		Rev <i>SD</i>
Date: Thursday, May 12, 2005		Sheet 36 of	44



Adapter

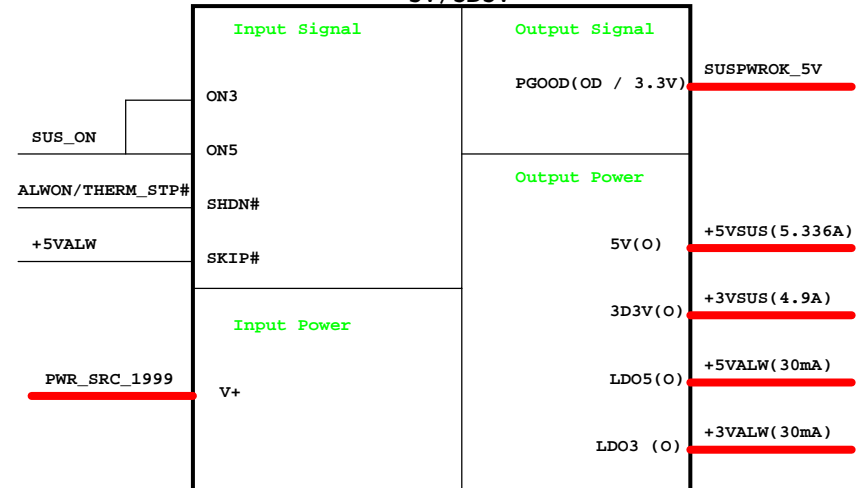


Charger MAX1909



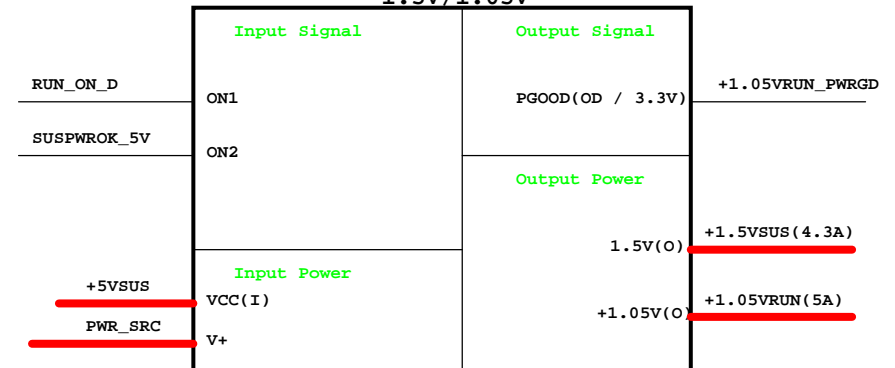
Max8734A

5V/3D3V



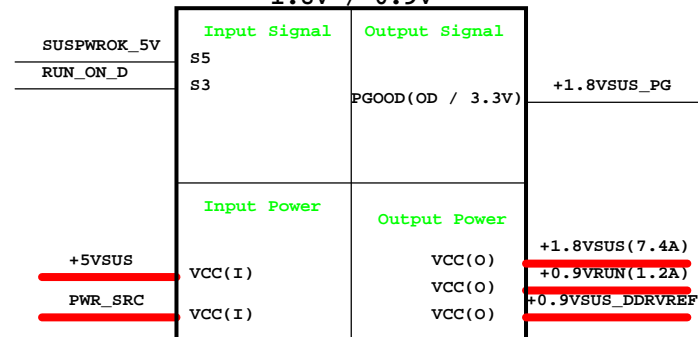
Max8743

1.5V/1.05V



TI51116

1.8V / 0.9V



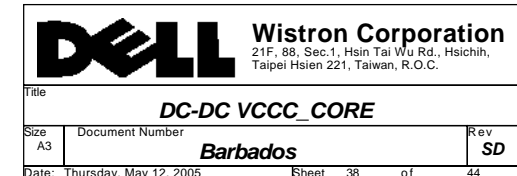
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Title			Power Block Diagram		
Size	Document Number	Rev			SD
A3		Barbados			
Date: Thursday, May 12, 2005			Sheet	37	of 44

	<i>Deeper</i>	<i>Deep</i>	<i>Active</i>
<i>DPRSLPVR</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>STP_CPU#</i>	<i>0</i>	<i>0</i>	<i>1</i>





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Title

+3V SRC_5V SUS

Size
A3

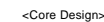
Document Number

Barbados

Rev
SD

Date: Thursday, May 12, 2005

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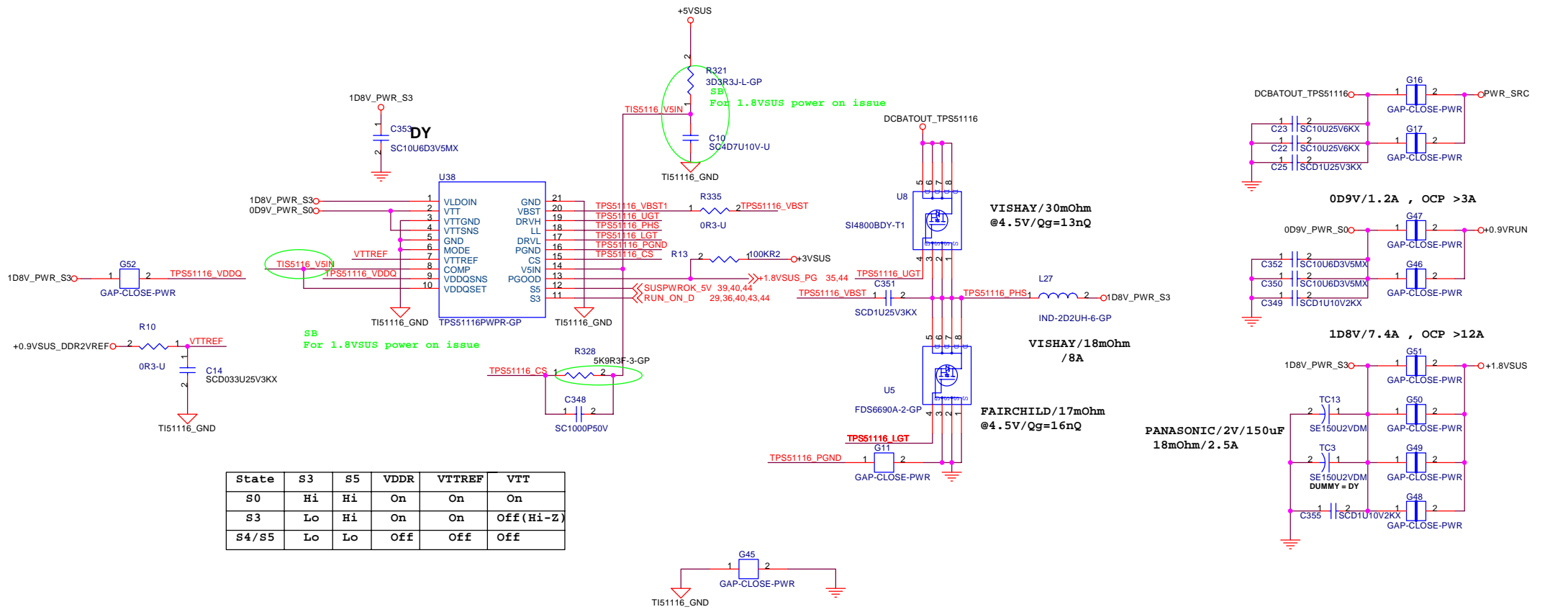


+1.5VSUS_1.05VRUN

Rev	SD
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44

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

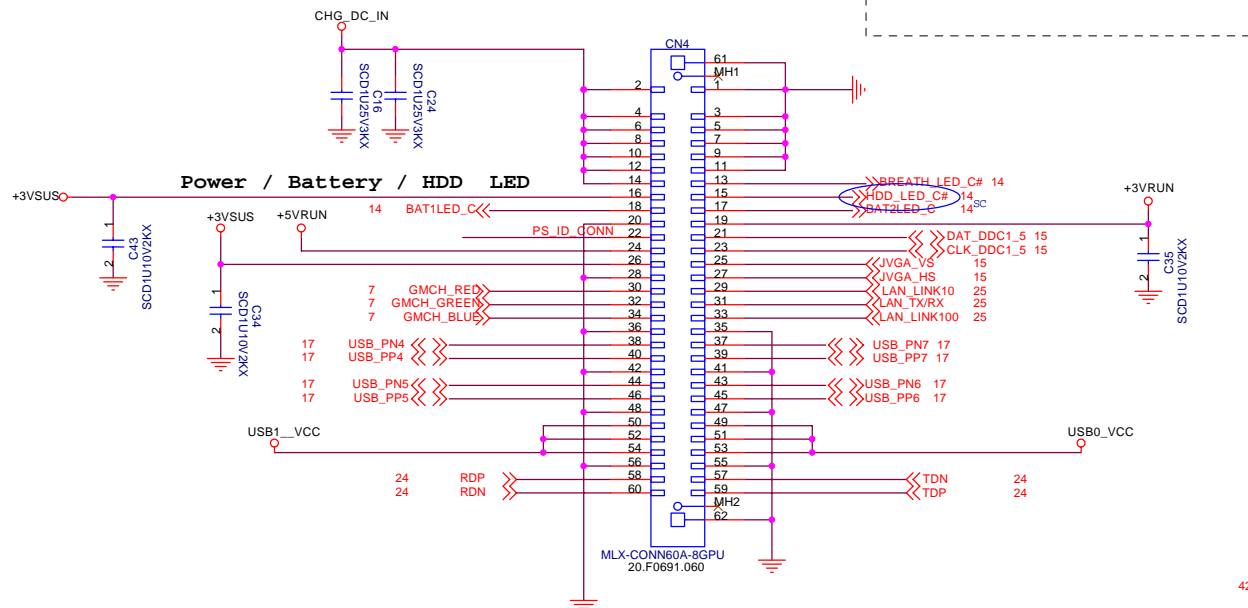
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **+1.8VSUS&0.9VRUN&DDR2_VREF**

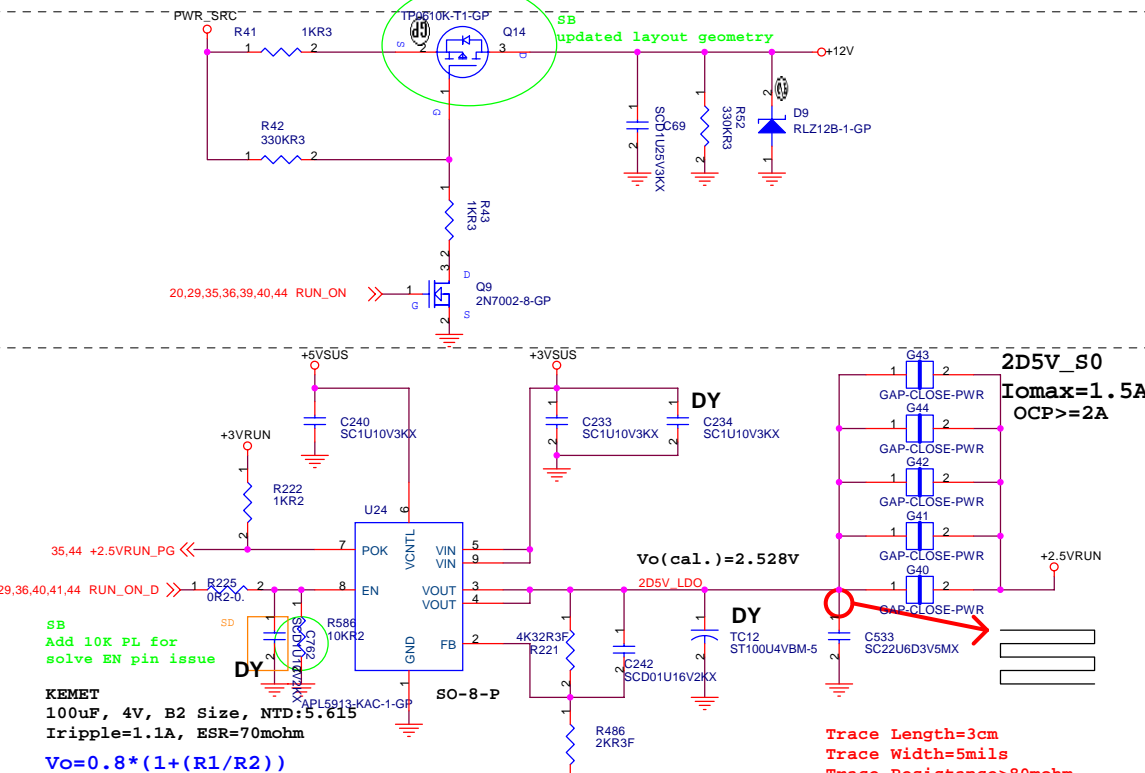
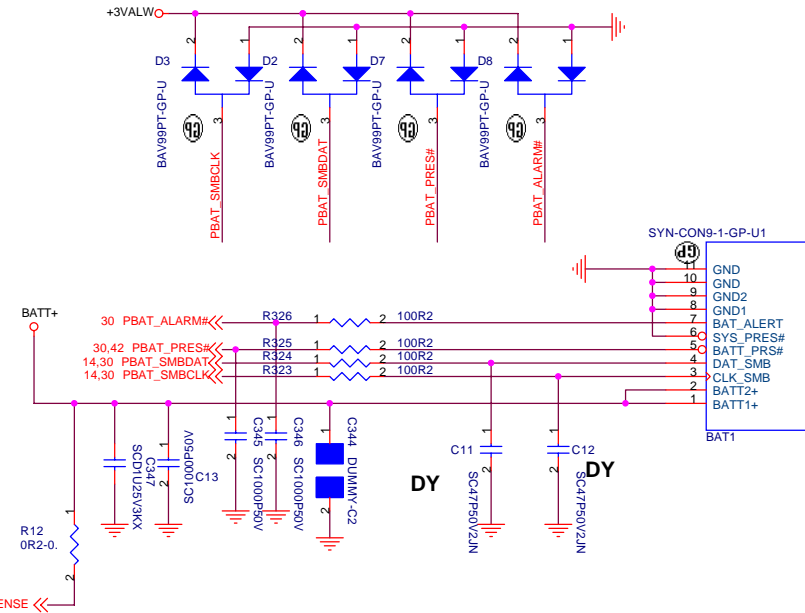
Size A3 Document Number: **Barbados** Rev: **SD**

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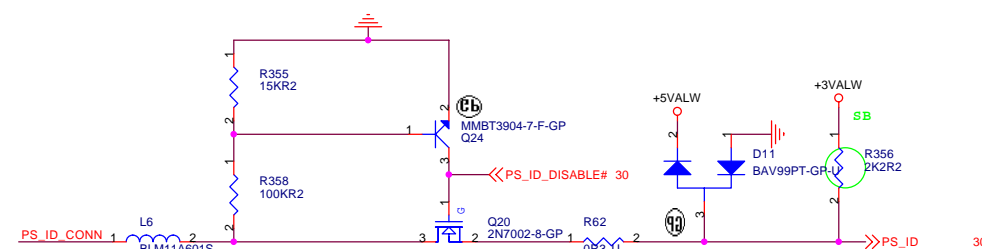
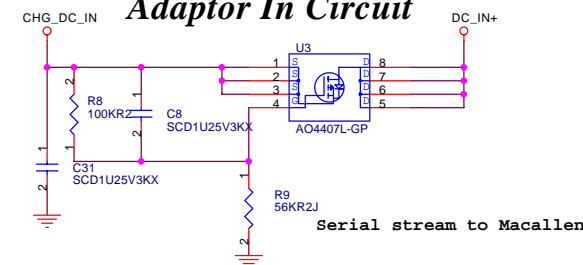
TV BD Conn



Battery Conn



Adaptor In Circuit



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Battery/TV/Adaptor Conn/+2.5VSUS**

Size: A3 Document Number: **Barbados** Rev: **SD**

Date: Thursday, May 12, 2005 Sheet: 43 of 44

